

# Clean Room Operations

# Manufacturing

- So far you've heard about solid mechanics, acoustics, and such
- How do we go about making practical devices?
- At mm and larger scales, manufacturing can be considered after the physics and design are finished
- At micro and smaller scales, **how** you make something is just as important as **why**

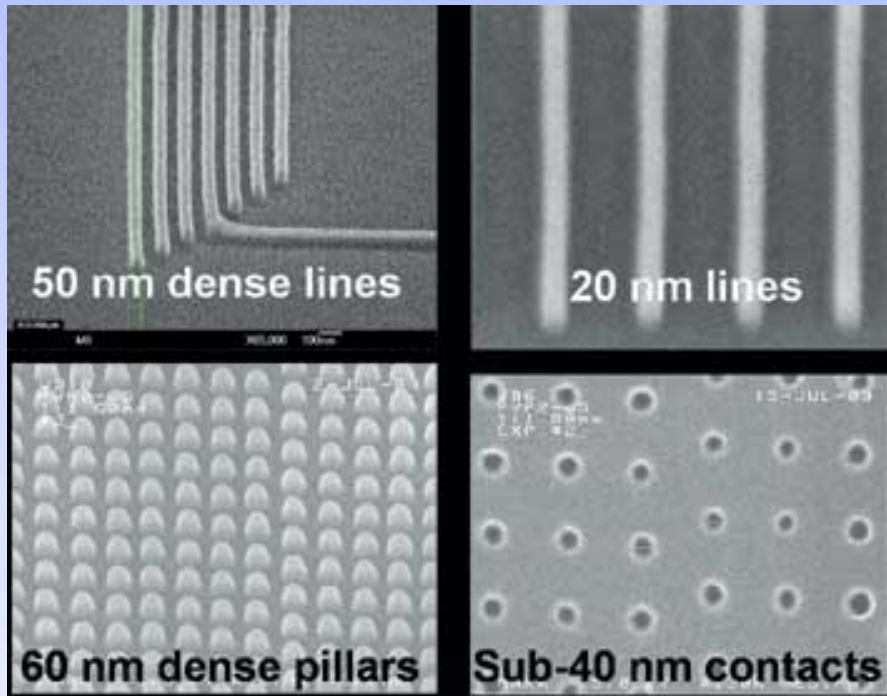
*Title slide: Imprint lithography has the potential to fabricate molecular-scale features. Lines only 50 and 20 nm wide (shown in micrographs, top left and top right), pillars 60 nm across (above left) and contacts just 40 nm wide (above right) were made with soft imprint nanophotolithography. So far, the only limit on the scale of features produced has been the ability to make templates with fine enough features. (from asme.org)*

# Objectives

- **Understand the importance of cleanliness and its definitions in the context of small manufacturing**
- **Understand the general process of machining at these scales**
- **Learn specific methods common to making micro and nanodevices to date**
- **Differentiate between different machining methods in their suitability and economy for specific purposes**

# Always Remember: What Seems Advanced Is Not So Much

- Nanophotolithography?

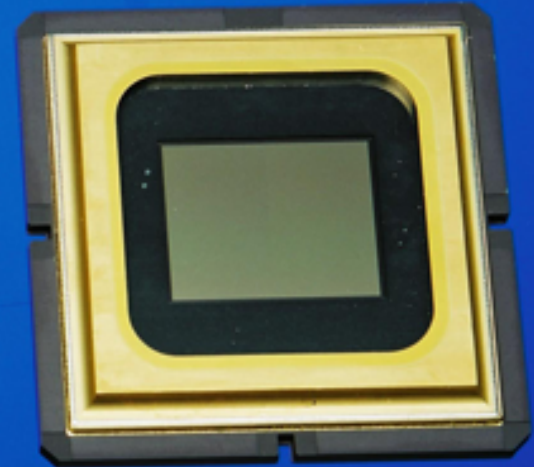
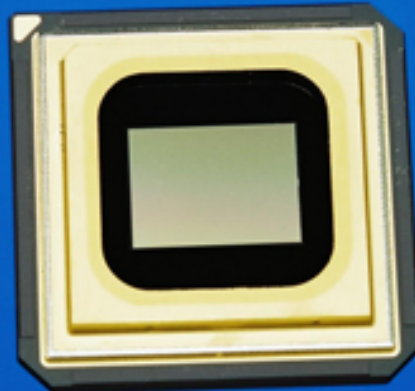


- 1834: Lithography (Honore Daumier. Transnonain Street. )



# Importance of Cleanliness

- Digital Light Projector (DLP) system from Texas Instruments
- Typical in video projector systems
- $1280 \times 1024 \times 3$  (RGB) = 3.9 million elements



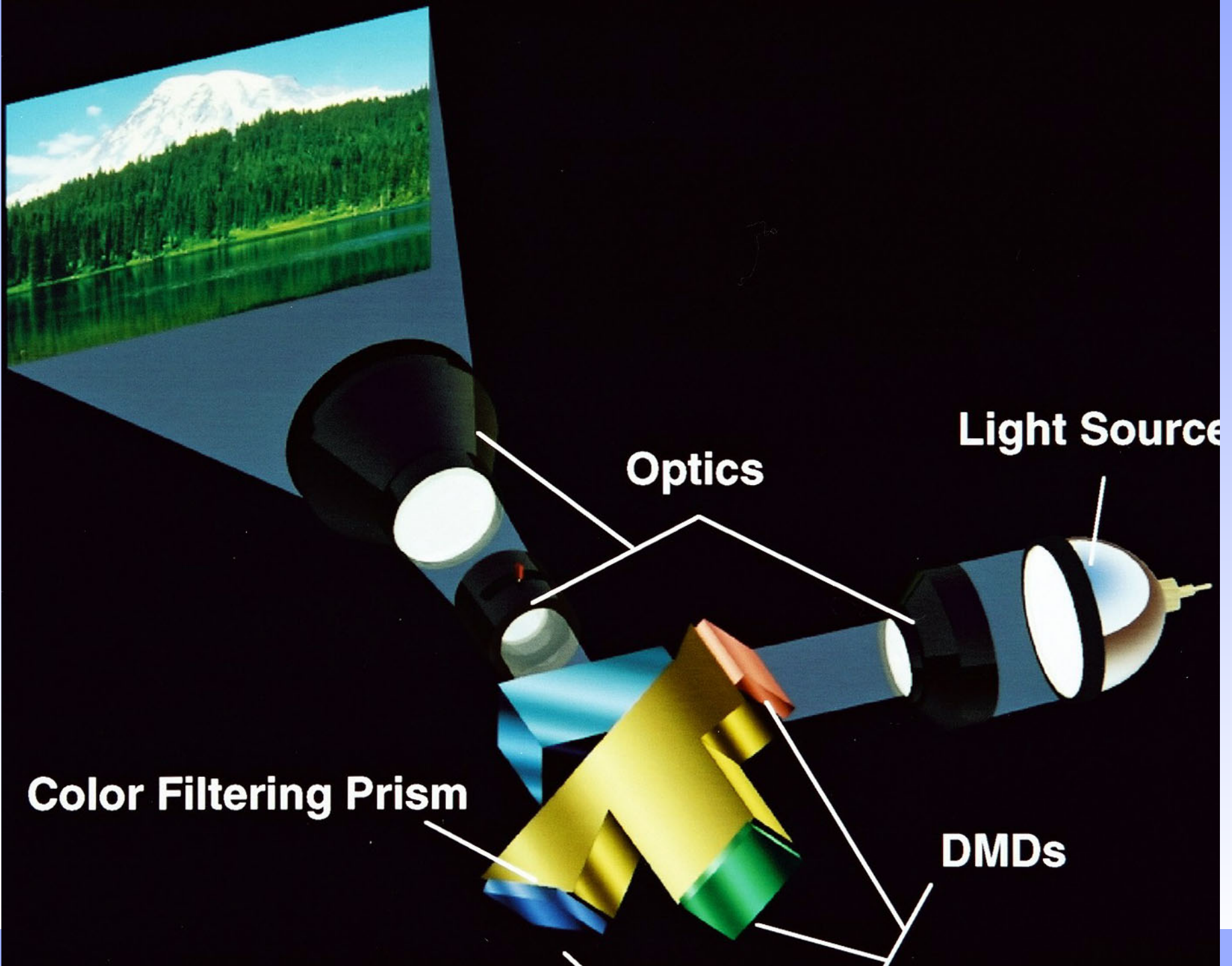


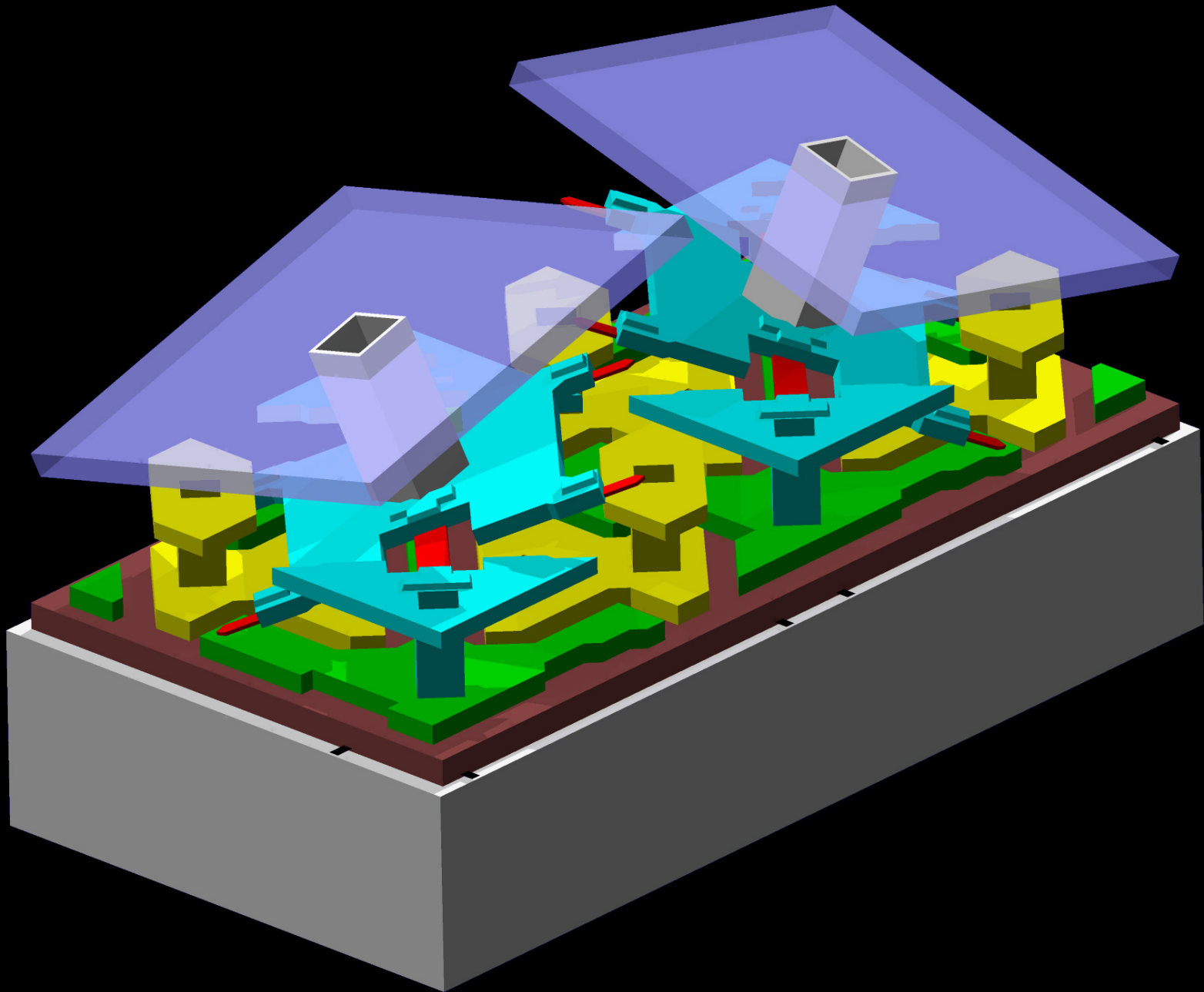
**Color Filtering Prism**

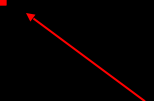
**Optics**

**Light Source**

**DMDs**



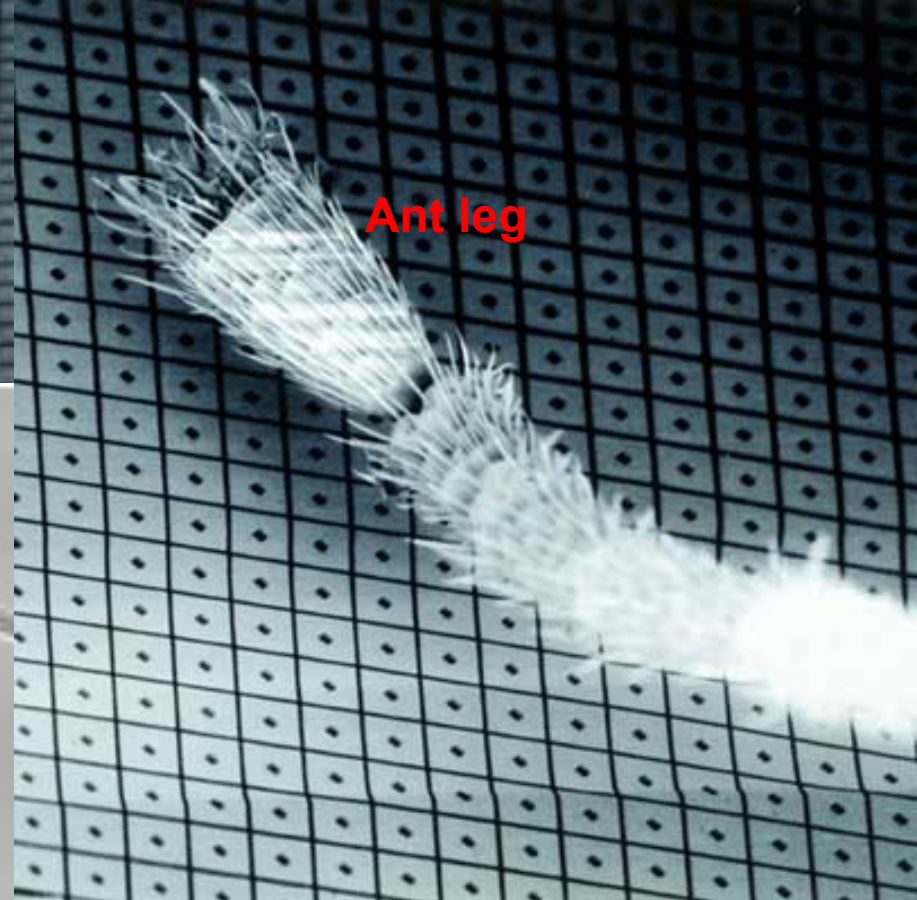


- 
- **1 in 3.9 million per device**
  - **Each device must be cheap: less than \$150**
  - **Each device should take less than a few minutes to make**





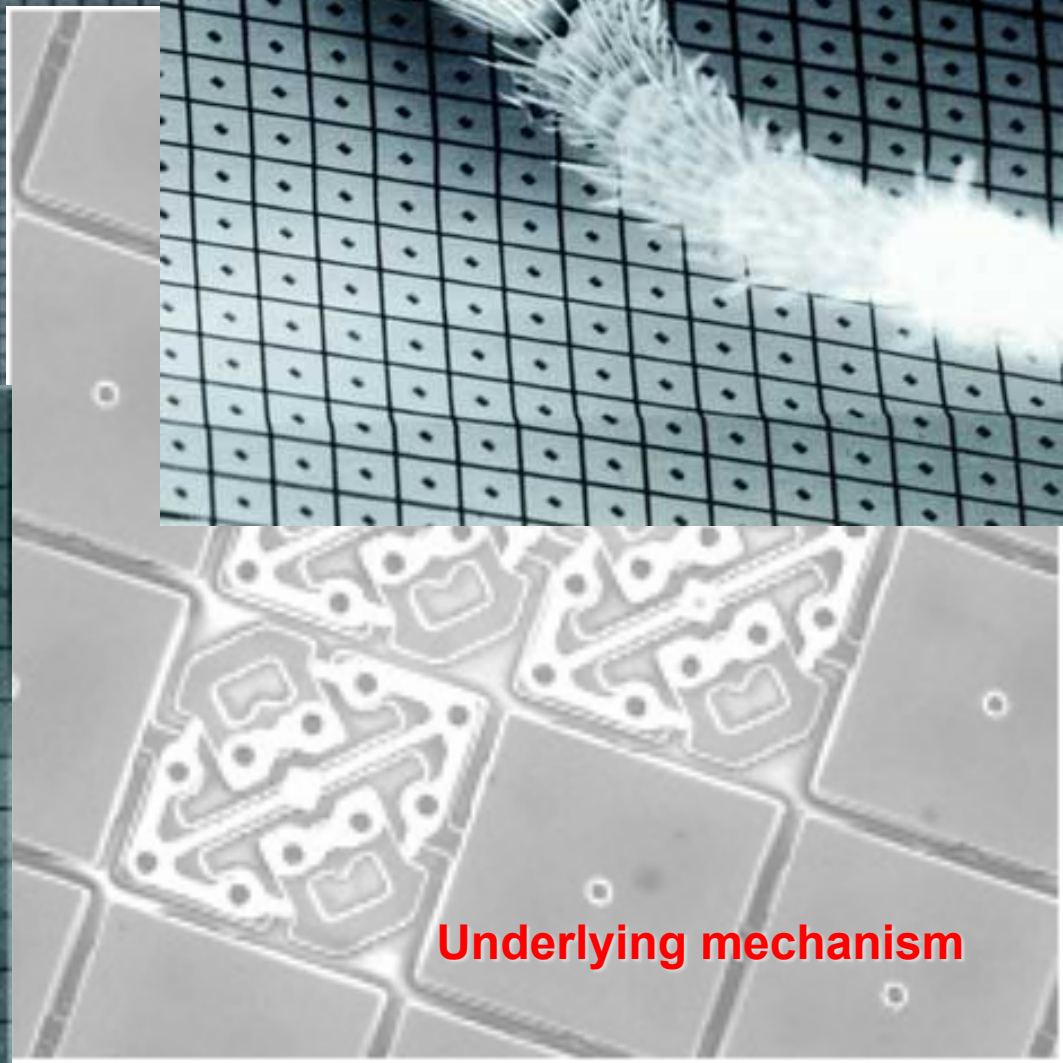
Pencil tip



Ant leg

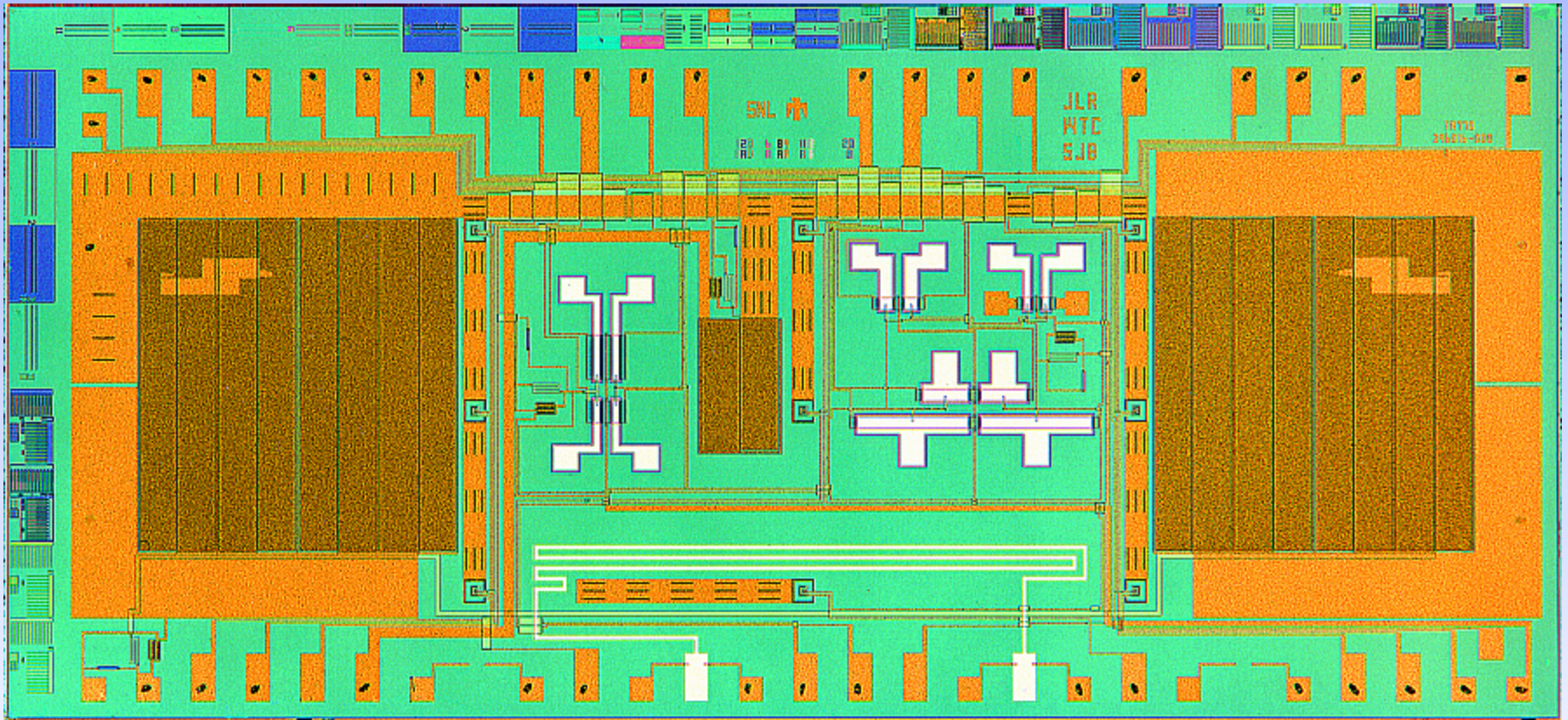


Salt



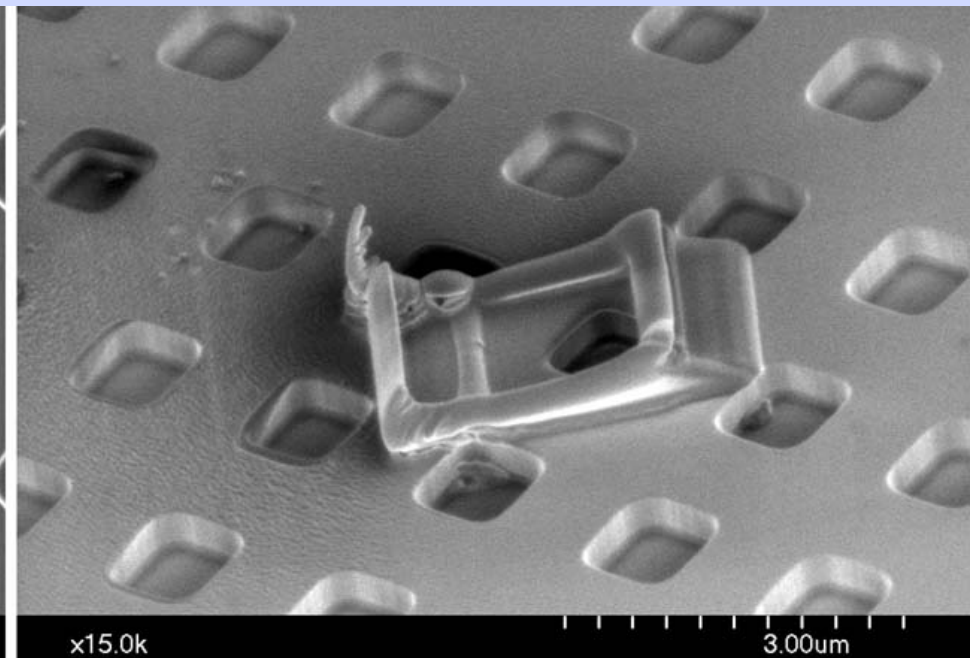
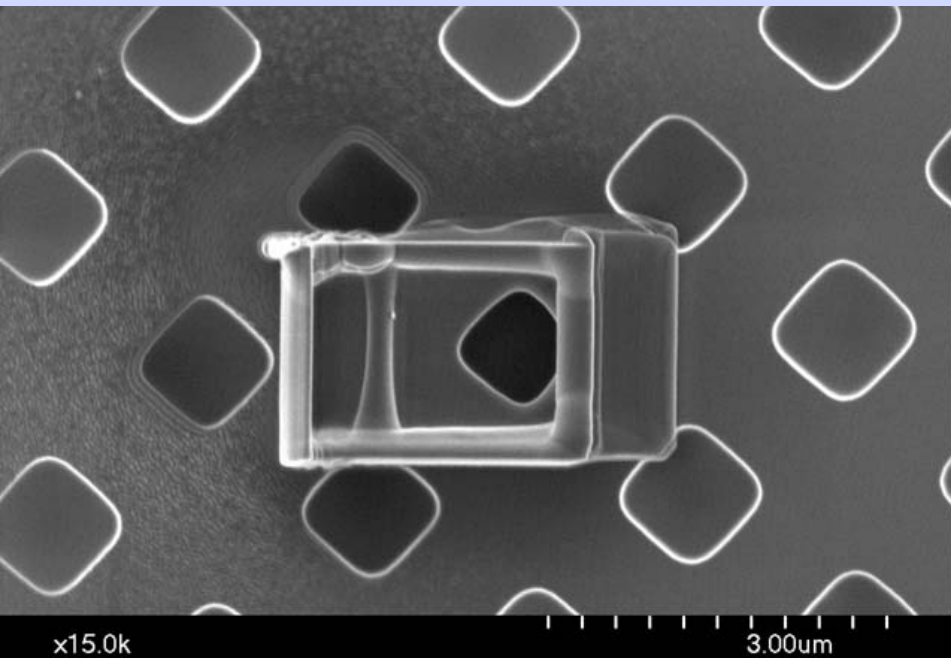
Underlying mechanism

# Complexity Example: Sandia Natl Labs: H2 sensor



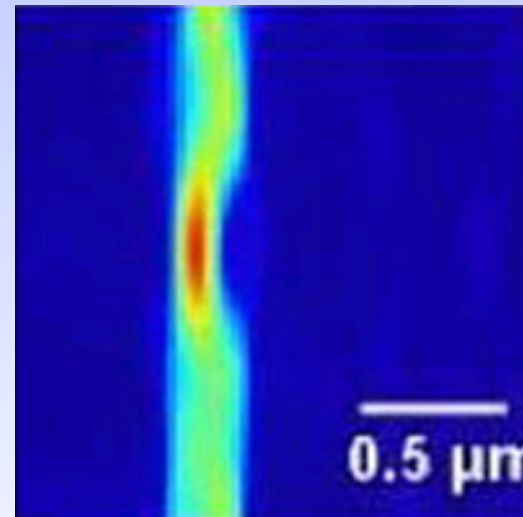
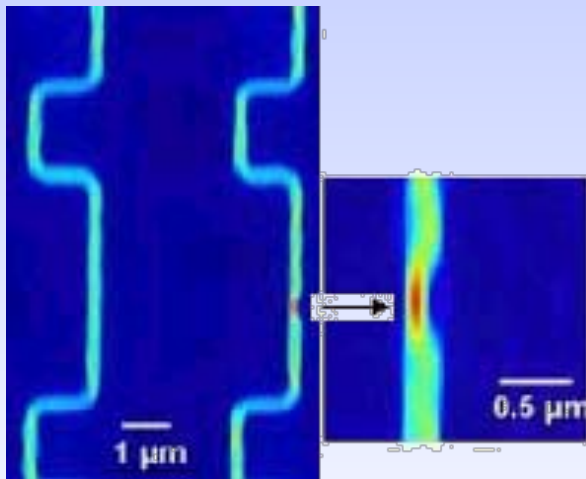
# Small-scale devices are

- **Characterized by their manufacturing similarities across copies: copy 1 is the same as copy 1000**
- **Used because they offer economies of scale**
- **Favored because they allow the use of physics at small scales**
- **A hassle to manufacture reliably for these reasons**

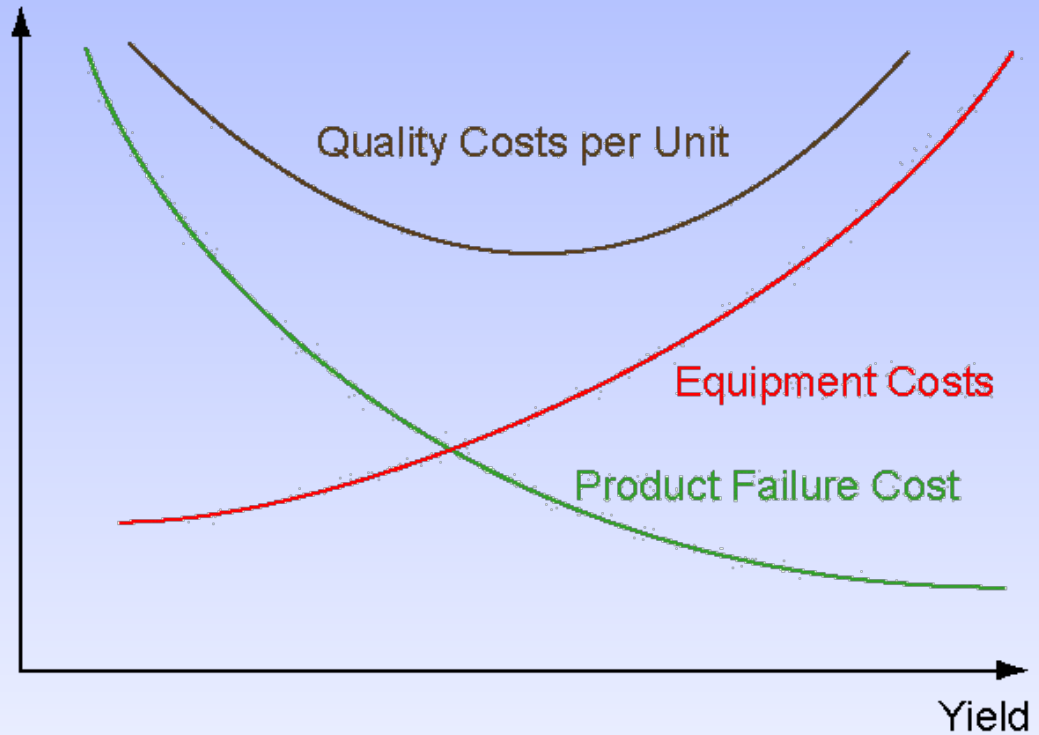
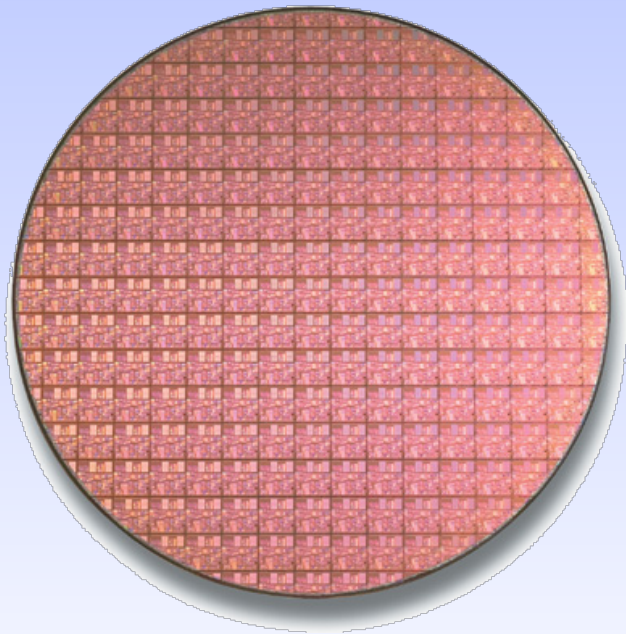


# “Insignificant” Flaws Add Expense

- Tiny flaw in one of two 0.25-micron metal wires in an integrated circuit chip.
- This detail shows the wire has a "mouse bite" along one of its edges, where the electrical current shows up as a tiny hot spot



# Quality Costs?



# How Clean Are We Talking?

- Suppose a dust particle were the size of a football
- Your clean room would have to be roughly the size of the earth to match the cleanliness of a class 1 clean room  
(Intel and other manufacturers routinely produce chips at levels beyond this)



# What Contaminants?

- **Air**
  - Handling and filtration equipment
  - Room geometry and construction
  - Clean room type
    - Turbulent
    - Laminar
- **Operators**
  - Movement: how and how fast
  - Hand, head, body positions
  - Clothing
  - Breathing
  - Cleanliness
- **Process**
  - Tools
  - Environment
  - Parts
  - Logistics
  - Actions
  - Waste disposal
  - Storage
- **Equipment**
  - Dust and fluid particle generation
  - Waste
  - Air flow

# What Materials Go in a Cleanroom?

- **Materials OK for clean room use**

- Stainless steel
- Aluminum
- Glass
- Most ceramics
- Many polymers, including
  - PTFE/Teflon
  - PP/Polypropylene
  - PVC/Polyvinylchloride
  - PVDF/Polyvinylidifluoride
  - PU/Polyurethane

- **Materials NEVER in a clean room**

- Zinc
- Copper
- Fibrous composites (glass, carbon, aramid, graphite)
- Wood
- Iron
- Lead
- Water (in a dream world, but in reality absolutely necessary)

***Never take a pencil and paper into a clean room!***



**People are covered by (hot stuffy)  
Tyvek suits with face masks and  
safety glasses**



**No one is standing OVER their work, but at arm's reach; everything is done slowly and from underneath or the side**



**Entire room is either stainless steel, glass, or plastic**





**Laminar Clean Room: Air in at top, out at bottom**



**Masks in storage to keep them clean  
(yes, you can get something dirty in  
a clean room)**

**No, he's not lazy, he's staying away from the bench**





**Yellow room color? From UV filters to prevent premature exposure of photoresists (see later)**

## Class 0 clean room







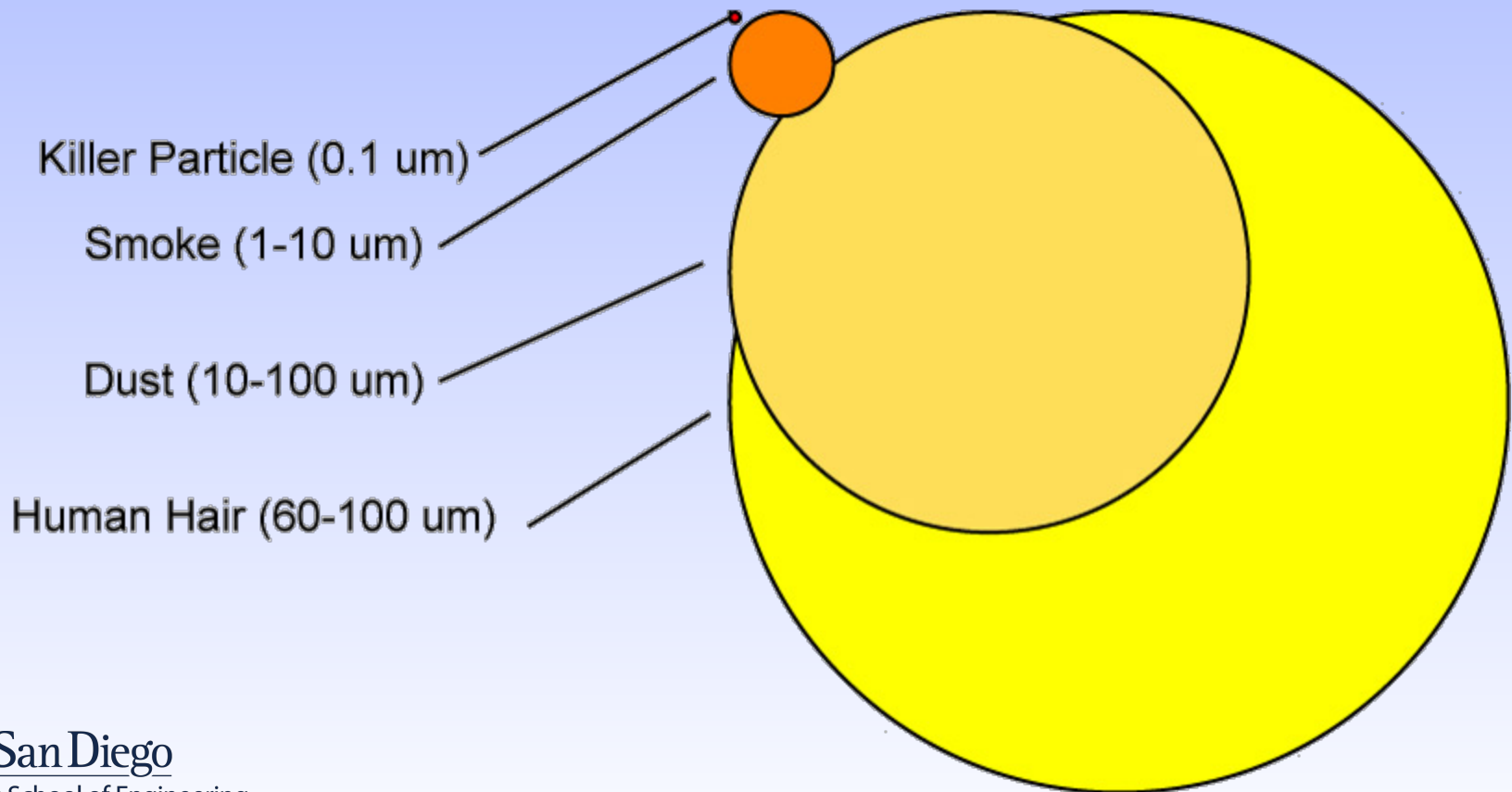
**Vents in solid floor:  
turbulent clean room**

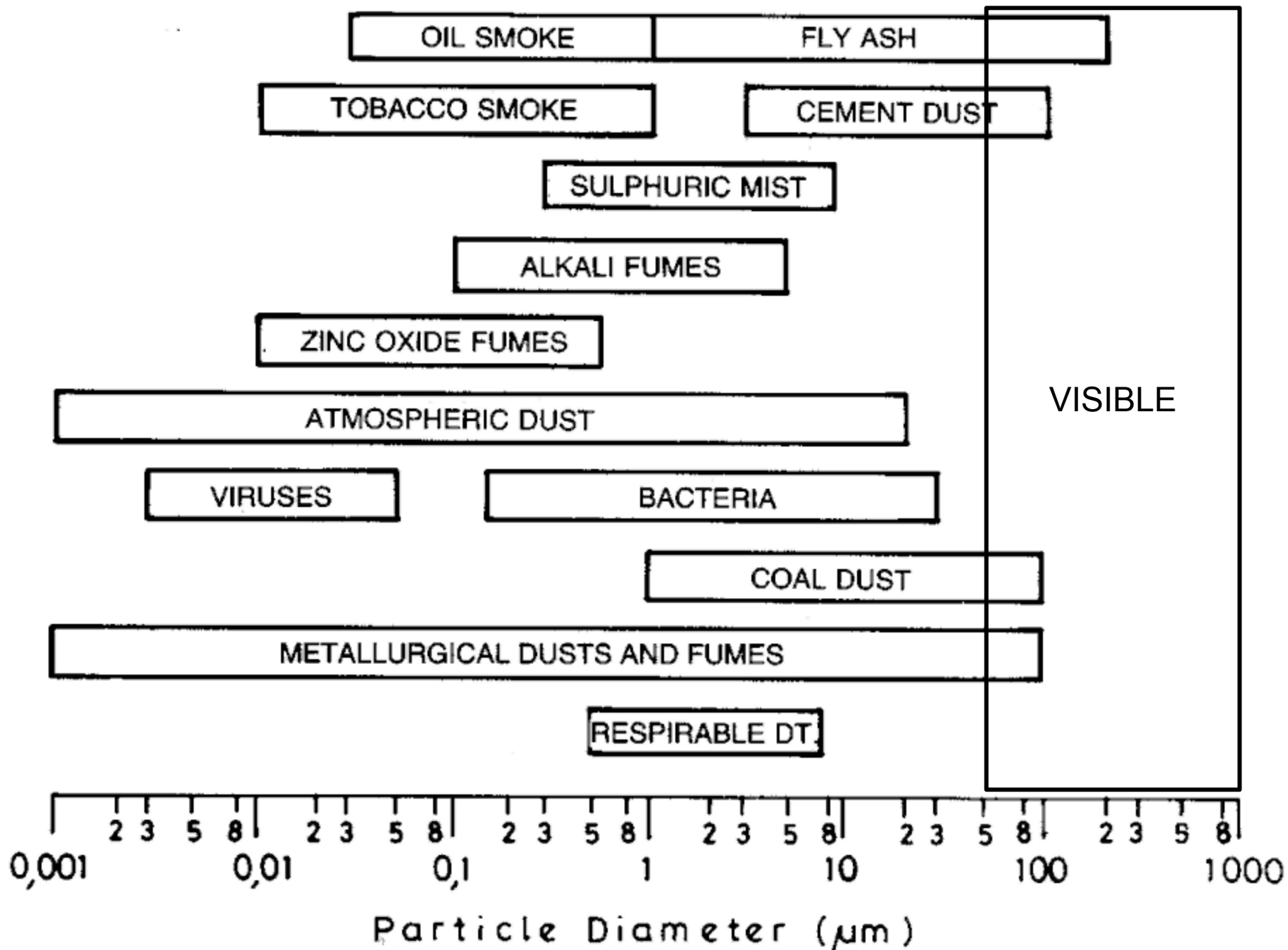
**But thorough clothing?  
A bit inconsistent...**

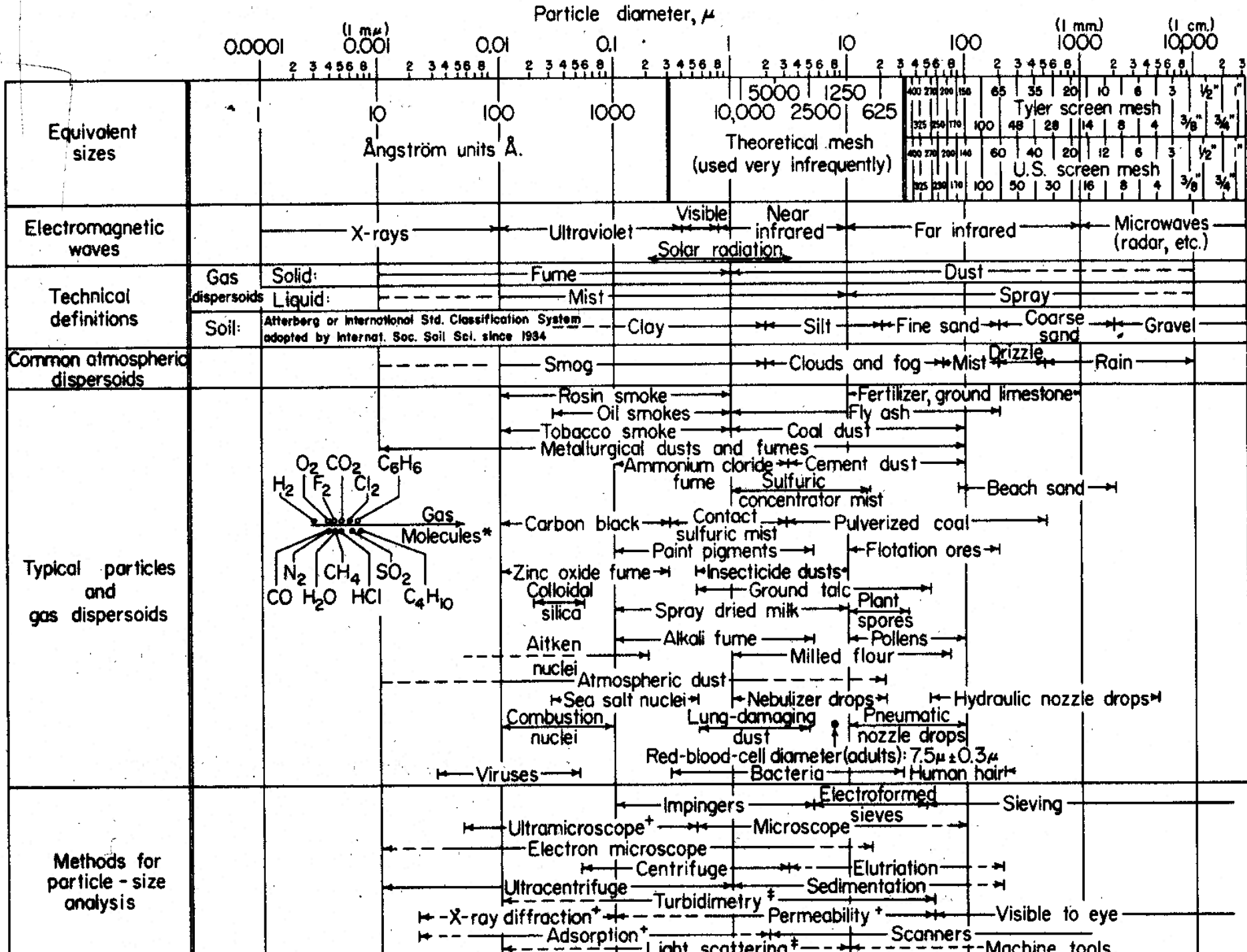
**~Class 1000 *university* clean  
room**

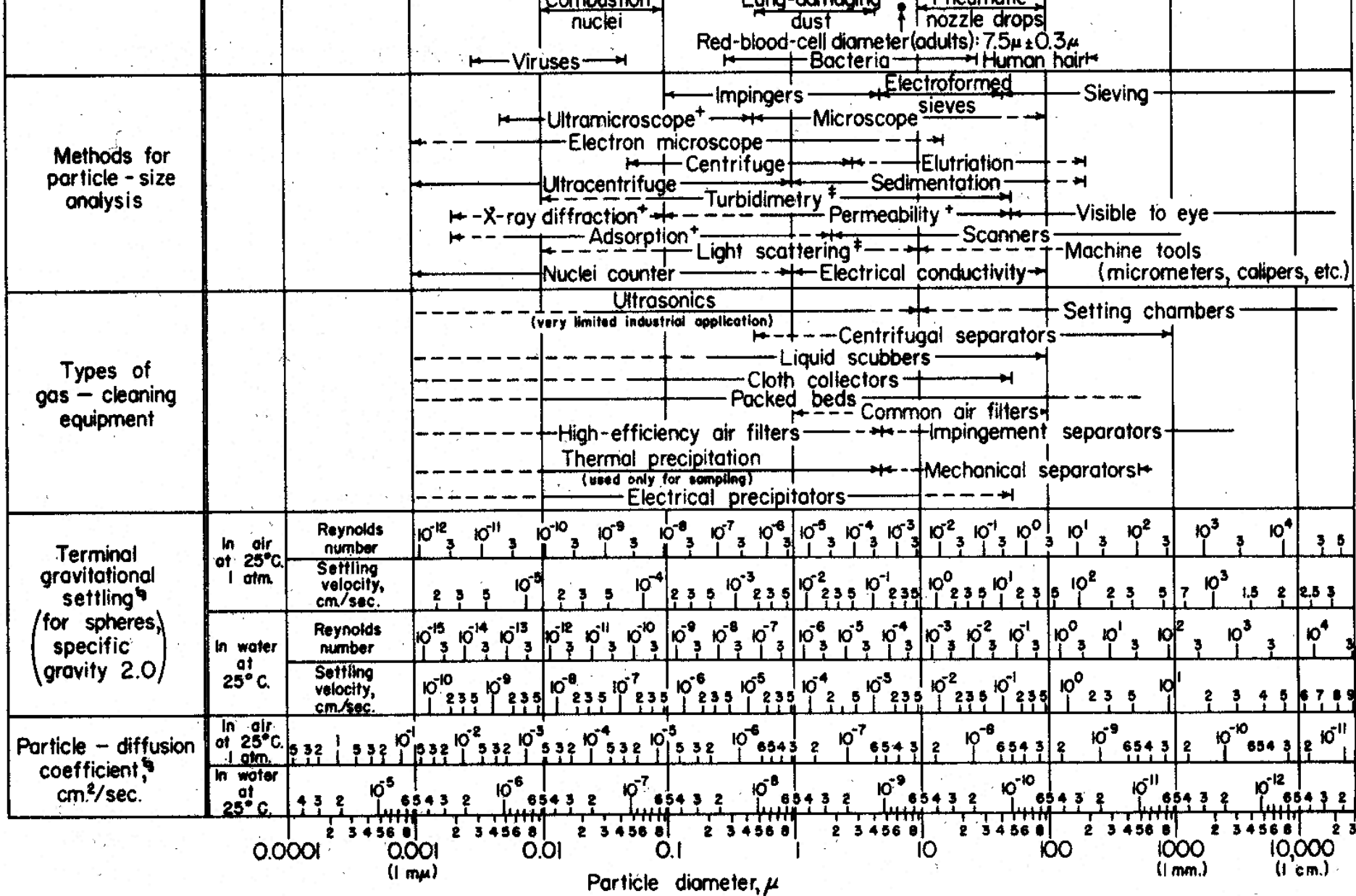
# The smallest particle is important...

Because you can't see it doesn't mean it isn't there...









\* Molecular diameters calculated from viscosity data at 0°C.

+ Furnishes average particle diameter but no size distribution.

‡ Size distribution may be obtained by special calibration.

§ Stokes-Cunningham factor included in values given for air but not included for water.

# US FED STD 209E cleanroom standards

- Traditional cleanroom definitions (popular)

Class	particle/ft <sup>3</sup>					
	0.1 μm	0.2 μm	0.3 μm	0.5 μm	1 μm	5 μm
<b>1</b>	35	7	3	<b>1</b>		
<b>10</b>	350	75	30	<b>10</b>	1	
<b>100</b>	3500	750	300	<b>100</b>	10	1
<b>1,000</b>				<b>1,000</b>	100	10
<b>10,000</b>				<b>10,000</b>	1,000	100
<b>100,000</b>				<b>100,000</b>	10,000	1,000

**Outside world, rainy day:** about class 1,000,000

**Dry day:** about class 10,000,000

# ISO 14644-1 cleanroom standards

- **The new standards as of 2001**

- 14644-1 through 14644-7: particulate clean rooms
- 14698-1 through 14698-3: bioparticulate clean rooms

Class	particle/m <sup>3</sup>					
	0.1 μm	0.2 μm	0.3 μm	0.5 μm	1 μm	5 μm
ISO 1	10	2				
ISO 2	100	24	10	4		
ISO 3	1,000	237	102	35	8	
ISO 4	10,000	2,370	1,020	352	83	
ISO 5	100,000	23,700	10,200	3,520	832	29
ISO 6	1,000,000	237,000	102,000	35,200	8,320	293
ISO 7				352,000	83,200	2,930
ISO 8				3,520,000	832,000	29,300
ISO 9				35,200,000	8,320,000	293,000

# Cleanroom Class Comparison

ISO 14644-1	FED STD 209E
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ISO 2	1
ISO 3	10
ISO 4	100
ISO 5	1,000
ISO 6	10,000
ISO 7	100,000



# Humans as Particle Sources

- **Bacteria**
  - Men: ~350 per sec-m<sup>3</sup>
  - Women: ~300 per sec-m<sup>3</sup>
- **>0.3um Particles, no protective clothing**
  - Men: ~4-5 particles/sec-m<sup>3</sup>
  - Women: ~2-3 particles/sec-m<sup>3</sup>
- **With protective clothing, both can be brought down to about 2 particles/m<sup>3</sup> per sec**
- **Smoking increases particle production to >10,000 particles/m<sup>3</sup> per exhalation for up to an hour after last cigarette**

ACTIVITY	PARTICLES/MIN (0.3 microns and larger)
Motionless (Standing or Seated)	100,000
Walking about 2 mph	5,000,000
Walking about 3.5 mph	7,000,000
Walking about 5 mph	10,000,000
Horseplay	100,000,000

# Typical Personal Clean Room Regulations

- 1. All personal items such as keys, watches, rings, matches, lighters and cigarettes should be stored in the personal locker outside the gowning room.
- 2. Valuable personal items such as wallets may be permitted in the cleanroom provided they are NEVER removed from beneath the cleanroom garments.
- 3. NO eating, smoking or gum chewing allowed inside the cleanroom.
- 4. Only garments approved for the cleanroom should be worn when entering.
- 5. NO cosmetics shall be worn in the cleanrooms. This includes: rouge, lipstick, eye shadow, eyebrow pencil, mascara, eye liner, false eye lashes, fingernail polish, hair spray, mousse, or the heavy use of aerosols, after shaves and perfumes.
- 6. Only approved cleanroom paper shall be allowed in the cleanroom.
- 7. Approved ball point pens shall be the only writing tool used.
- 8. Use of paper or fabric towels are prohibited. Use of hand dryers equipped with HEPA filters are suggested.
- 9. Gloves or finger cots should not be allowed to touch any item or surface that has not been thoroughly cleaned.
- 10. Only approved gloves, finger cots (powder-free), pliers, tweezers should be used to handle product. Finger prints can be a major source of contamination on some products.
- 11. Solvent contact with the bare skin should be avoided. They can remove skin oils and increase skin flaking.
- 12. Approved skin lotions or lanolin based soaps are sometimes allowed. These can reduce skin flaking.
- 13. All tools, containers and fixtures used in the cleaning process should be cleaned to the same degree as the cleanroom surfaces. All of these items are a source of contamination.
- 14. NO tool should be allowed to rest on the surface of a bench or table. It should be placed on a cleanroom wiper.
- 15. Only cleanroom approved wipers are allowed to be used. The wipers must be approved for the Class of cleanroom being cleaned.
- 16. ALL equipment, materials and containers introduced into a sterile facility must be subjected to stringent sterilization prior to entrance.
- 17. NO ONE who is physically ill, especially with respiratory or stomach disorders, may enter a sterile room. This is a good practice in any cleanroom environment.

# Manufacturing

# General Machining Process

1. **Base:** the *substrate*
2. **Clean**
3. **Treat**
4. **“Differentiate”** (make some parts of the object *different* than the rest)
5. **Rinse and Repeat** steps 3, 4 (and 2 where necessary)
6. **Integrate**

# 1. Base: *Substrate*

- The substrate provides a surface to work on, and has purity, chemical, EM, optical, or other useful characteristics
- Purity → single crystal or rarely, polycrystalline, amorphous or metallic materials
- Produced via Czochralski or similar processes (crystal pulling from molten bath in crucible while turning)
- Items at right are *single crystals!*



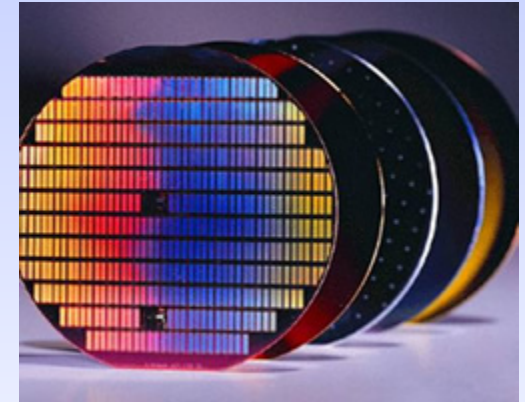
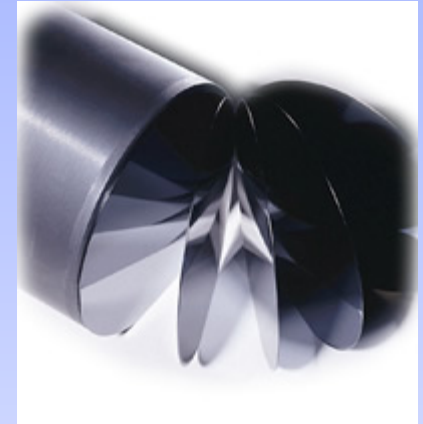
Silicon



Lithium  
Niobate

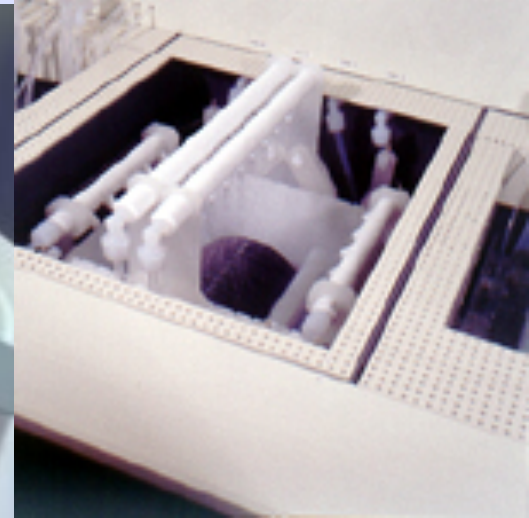
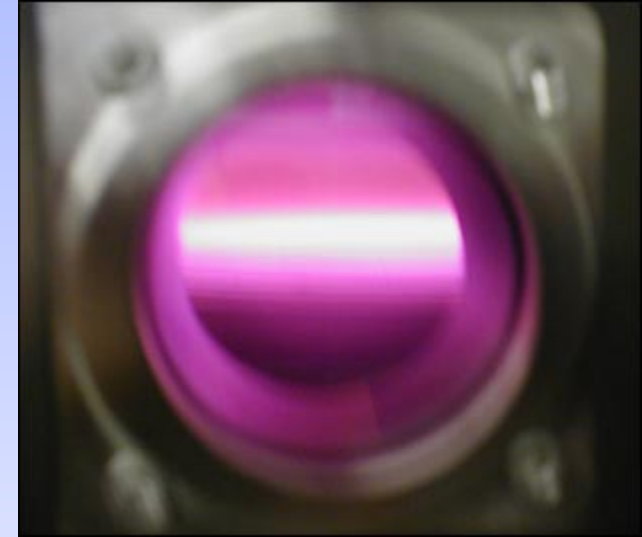
# 1. Base: *Substrate (cont'd)*

- **Once you have the substrate, cutting it is the next task**
- **Wafers obtained by**
  1. diamond saw cutting
  2. polishing
- **The wafers are used to support the subsequent steps**
- **Metal, ceramic, or polymer substrates may also be used**



# 2. Cleaning

- The wafers must be cleaned after manufacture
- The kind of cleaning depends on the process that will be used to manufacture something from it later
  - Acetone/Alcohol/DI Water/N<sub>2</sub>
  - Piranha process
  - Plasma etch
- **Critically important**



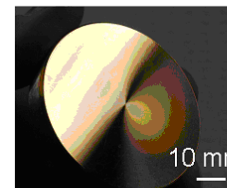
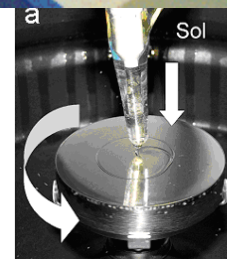
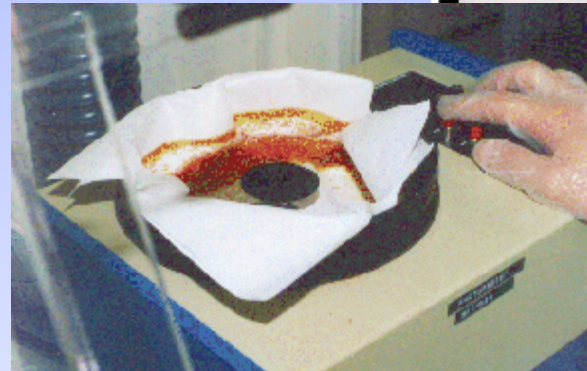
# Cleaning Example Process

- Standard degrease:
  - 2-5 min. soak in acetone with ultrasonic agitation
  - 2-5 min. soak in methanol with ultrasonic agitation
  - 2-5 min. soak in DI H<sub>2</sub>O with ultrasonic agitation
  - 30 sec. rinse under free flowing DI H<sub>2</sub>O
  - spin rinse dry for wafers; N<sub>2</sub> blow off dry for tools and chucks
- For particularly troublesome grease, oil, or wax stains:
  - Start with 2-5 min. soak in 1,1,1-trichloroethane (TCA) or
  - Trichloroethylene (TCE) with ultrasonic agitation prior to acetone

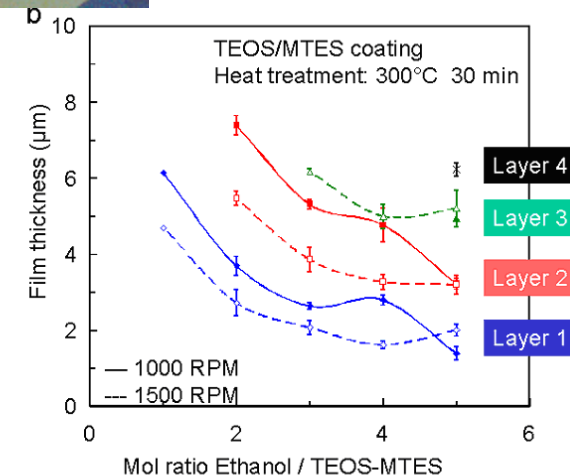


# 3. Treatment

- **Oxidize/reduce surface or entire wafer**
  - Si → SiO<sub>2</sub> 20nm thick layer on Si wafer
  - LiNbO<sub>3</sub> → reduced LiNbO<sub>3</sub> for reduced pyroelectricity
- **Coat surface of wafer**
  - metal
    - sputter
    - electrodeposit
  - polymer
    - spin-coat
    - dip-coat



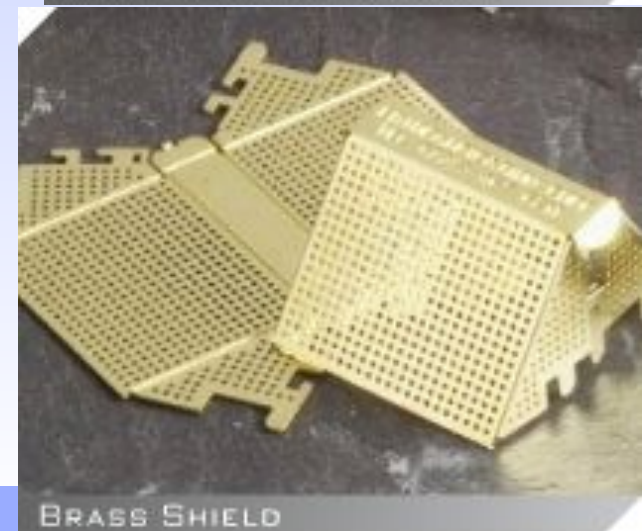
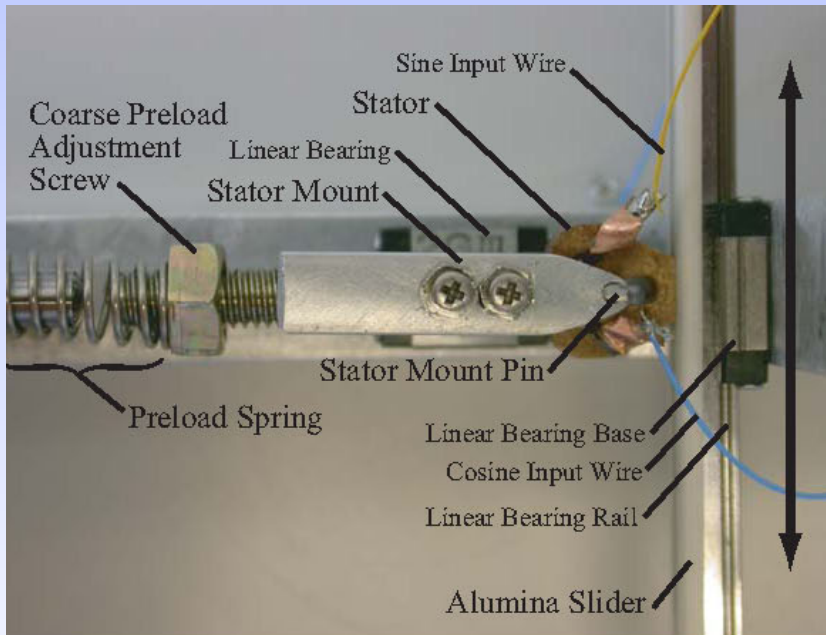
Spin coating for Machining



S. Middleman and A.K. Hochberg *Process Engineering Analysis in Semiconductor Device Fabrication*, McGraw-Hill, p. 313 (1993)

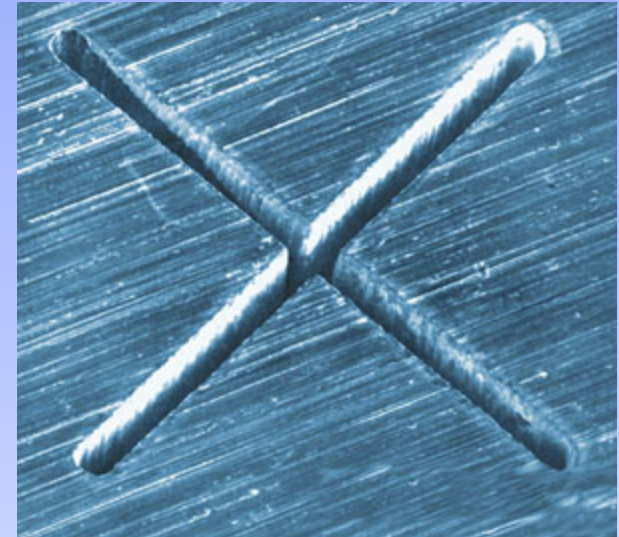
# 4. “Differentiate”

- **Traditional machining + x**
  - Drill
  - Lathe
  - Chemical etch



# 4. “Differentiate”

- Traditional machining + x
- Irradiate
  - pinpoint
  - flood with mask
  - flood without mask
- Pinpoint → laser irradiation
  - Heat generation cutting/welding
    - CO2 (577-585 nm, IR, others)
    - Nd:YAG (1064nm)
  - XeF 486 nm excimer (correctly “exciplex” laser, or “cold”): cuts via bond breakage
  - AVIA 266, 355, 532 nm UV exciplex



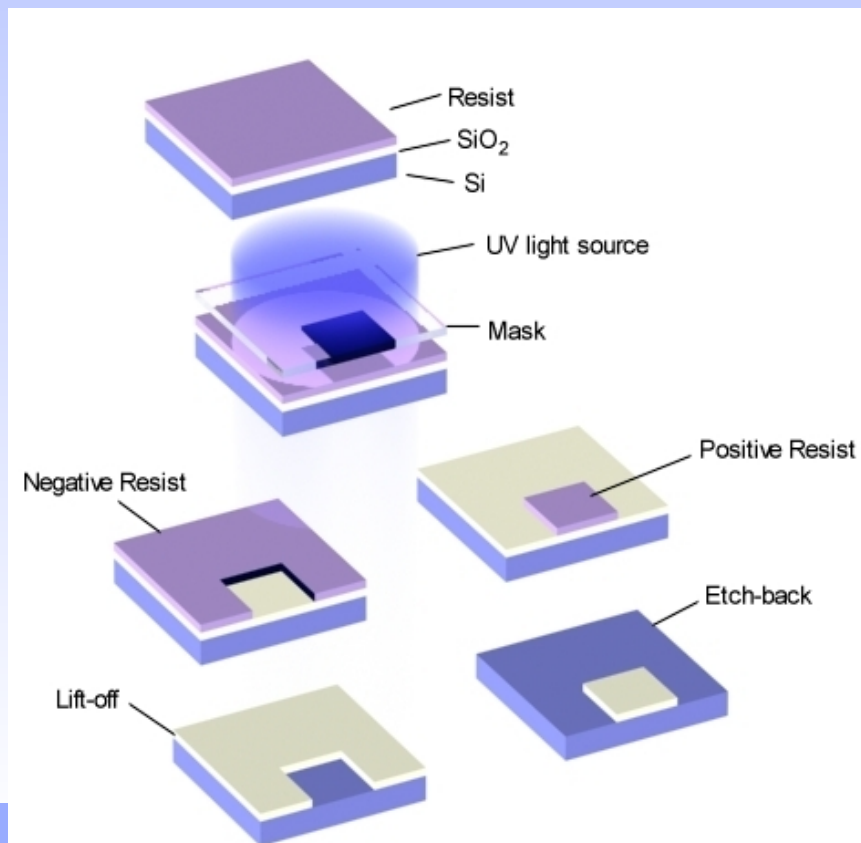
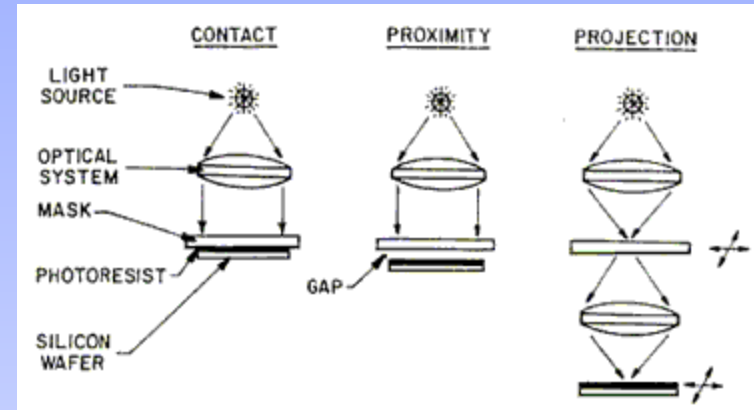
Spinneret cutting 40um



Gear component welding

# 4. “Differentiate”

- Traditional machining + x
- Irradiate
  - pinpoint
  - flood with mask
  - flood without mask
- Pinpoint → laser irradiation
- Flood with mask → lithography
  - Visible, UV, deep UV, x-ray photolithography
  - requires coating of photosensitive polymer and mask to make pattern
  - Mask is quartz, silica, or even graphite with stainless steel or beryllium pattern to block radiation
- Flood without mask → surface treatment



# 5. Rinse and Repeat

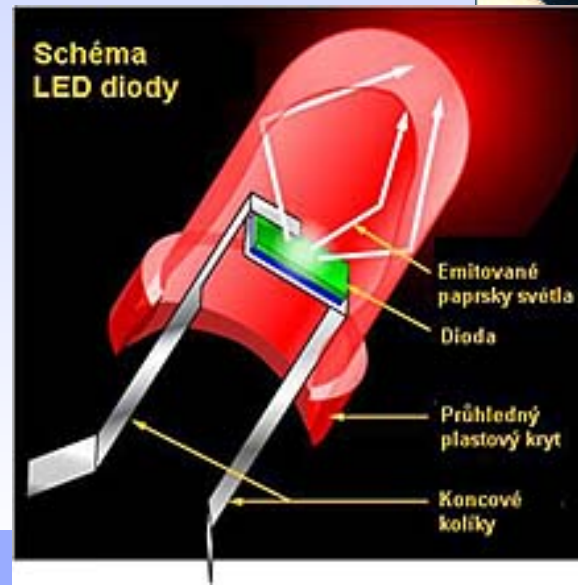
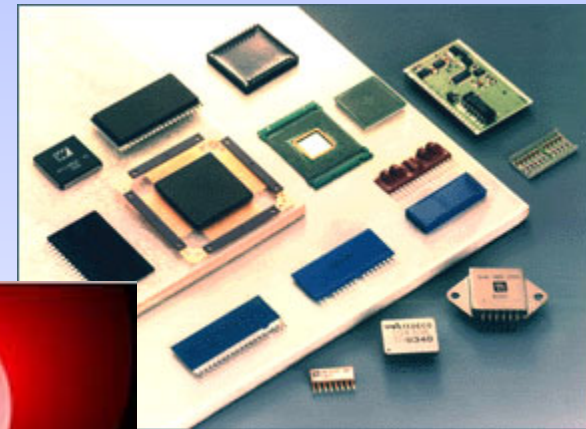
- Clean wafer *and/or*
- Clean areas exposed to radiation *or*
- Clean areas not exposed to radiation
- Prepare for treatment and or complete cleaning again
- If finished, proceed to *integration*

# 6. Integrate

- Having a micro/nanodevice, while nice, is insufficient
- Doing something with it requires
  - external connections
    - EM
    - optical
    - structural (fluid/solid)
    - thermal
    - chemical
    - quantum
  - protection (environment)
- Much more difficult than it sounds



Figure 6. iMEMS accelerometer in surface mount package



# **From Sand to Silicon**

## **“Making of a Chip”**

### **Illustrations**

**May 2009**

# Sand / Ingot



## **Sand**

With about 25% (mass) Silicon is - after Oxygen - the second most frequent chemical element in the earth's crust. Sand - especially Quartz - has high percentages of Silicon in the form of Silicon dioxide ( $\text{SiO}_2$ ) and is the base ingredient for semiconductor manufacturing.



## **Melted Silicon -**

*scale: wafer level (~300mm / 12 inch)*  
Silicon is purified in multiple steps to finally reach semiconductor manufacturing quality which is called Electronic Grade Silicon. Electronic Grade Silicon may only have one alien atom every one billion Silicon atoms. In this picture you can see how one big crystal is grown from the purified silicon melt. The resulting mono crystal is called Ingot.

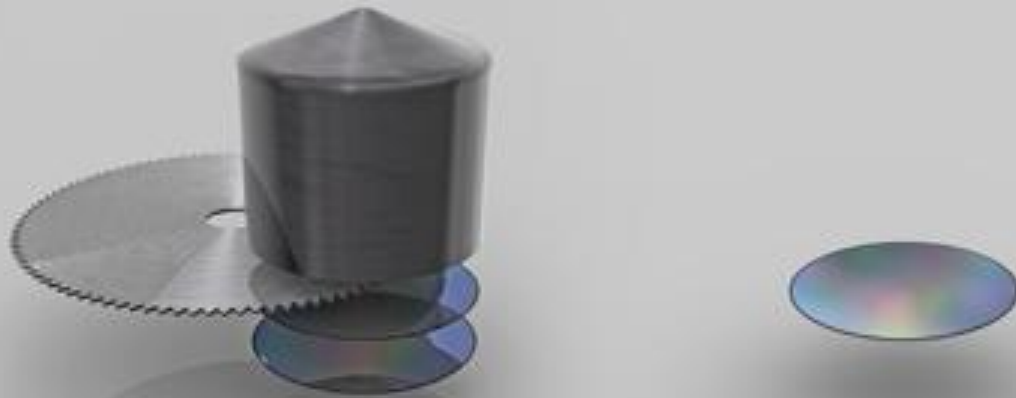


## **Mono-crystal Silicon Ingot -**

*scale: wafer level (~300mm / 12 inch)*  
An ingot has been produced from Electronic Grade Silicon. One ingot weights about 100 kilograms (=220 pounds) and has a Silicon purity of 99.9999%.



# Ingots / Wafer



## *Ingots Slicing -*

*scale: wafer level (~300mm / 12 inch)*

The Ingot is cut into individual silicon discs called wafers.

## **Wafer -**

scale: wafer level (~300mm / 12 inch)

The wafers are polished until they have flawless, mirror-smooth surfaces. Intel buys those manufacturing ready wafers from third party companies. Intel's highly advanced 45nm High-K/Metal Gate process uses wafers with a diameter of 300 millimeter (~12 inches). When Intel first began making chips, the company printed circuits on 2-inch (50mm) wafers. Now the company uses 300mm wafers, resulting in decreased costs per chip.

# Photo Lithography



## **Applying Photo Resist -**

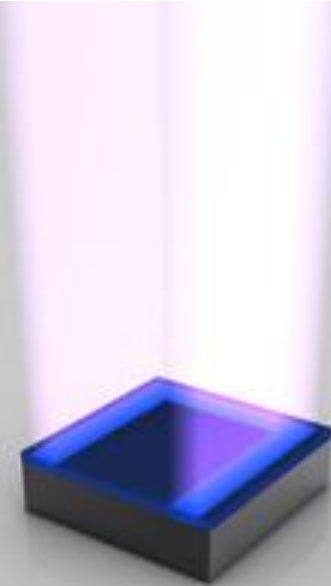
*scale: wafer level (~300mm / 12 inch)*

The liquid (blue here) that's poured onto the wafer while it spins is a photo resist finish similar as the one known from film photography. The wafer spins during this step to allow very thin and even application of this photo resist layer.

## **Exposure -**

*scale: wafer level (~300mm / 12 inch)*

The photo resist finish is exposed to ultra violet (UV) light. The chemical reaction triggered by that process step is similar to what happens to film material in a film camera the moment you press the shutter button. The photo resist finish that's exposed to UV light will become soluble. The exposure is done using masks that act like stencils in this process step. When used with UV light, masks create the various circuit patterns on each layer of the microprocessor. A lens (middle) reduces the mask's image. So what gets printed on the wafer is typically four times smaller linearly than the mask's pattern.

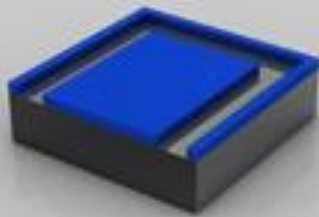


## **Exposure -**

*scale: transistor level (~50-200nm)*

Although usually hundreds of microprocessors are built on a single wafer, this picture story will only focus on a small piece of a microprocessor from now on - on a transistor or parts thereof. A transistor acts as a switch, controlling the flow of electrical current in a computer chip. Intel researchers have developed transistors so small that about 30 million of them could fit on the head of a pin.

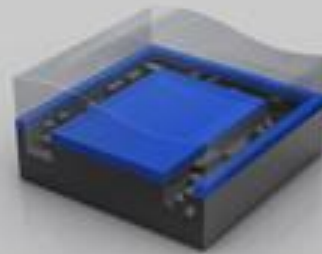
# Etching



## *Washing off of Photo Resist -*

*scale: transistor level (~50-200nm)*

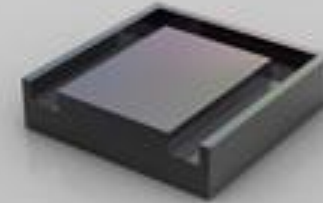
The gooey photo resist is completely dissolved by a solvent. This reveals a pattern of photo resist made by the mask.



## *Etching -*

*scale: transistor level (~50-200nm)*

The photo resist is protecting material that should not be etched away. Revealed material will be etched away with chemicals.

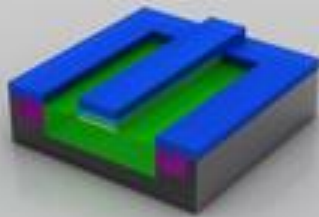


## *Removing Photo Resist -*

*scale: transistor level (~50-200nm)*

After the etching the photo resist is removed and the desired shape becomes visible.

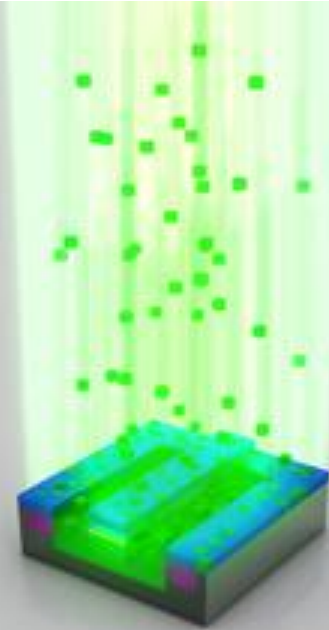
# Ion Implantation



## *Applying Photo Resist -*

*scale: transistor level (~50-200nm)*

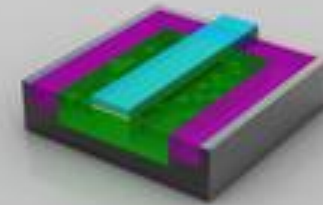
There's photo resist (blue color) applied, exposed and exposed photo resist is being washed off before the next step. The photo resist will protect material that should not get ions implanted.



## *Ion Implantation -*

*scale: transistor level (~50-200nm)*

Through a process called ion implantation (one form of a process called doping), the exposed areas of the silicon wafer are bombarded with various chemical impurities called ions. Ions are implanted in the silicon wafer to alter the way silicon in these areas conducts electricity. Ions are shot onto the surface of the wafer at very high speed. An electrical field accelerates the ions to a speed of over 300,000 km/h (~185,000 mph)

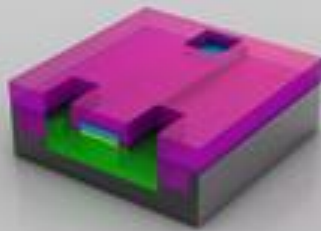


## *Removing Photo Resist -*

*scale: transistor level (~50-200nm)*

After the ion implantation the photo resist will be removed and the material that should have been doped (green) has alien atoms implanted now (notice slight variations in color)

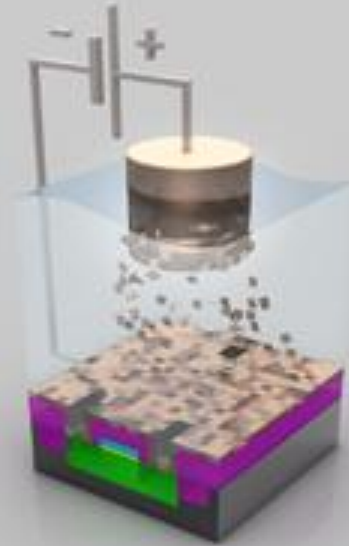
# Metal Deposition



## *Ready Transistor -*

*scale: transistor level (~50-200nm)*

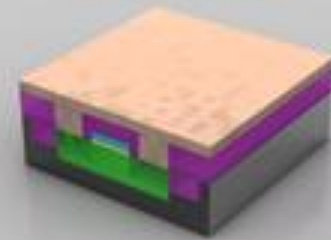
This transistor is close to being finished. Three holes have been etched into the insulation layer (magenta color) above the transistor. These three holes will be filled with copper which will make up the connections to other transistors.



## *Electroplating -*

*scale: transistor level (~50-200nm)*

The wafers are put into a copper sulphate solution as this stage. The copper ions are deposited onto the transistor thru a process called electroplating. The copper ions travel from the positive terminal (anode) to the negative terminal (cathode) which is represented by the wafer.

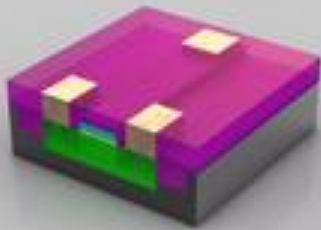


## *After Electroplating -*

*scale: transistor level (~50-200nm)*

On the wafer surface the copper ions settle as a thin layer of copper.

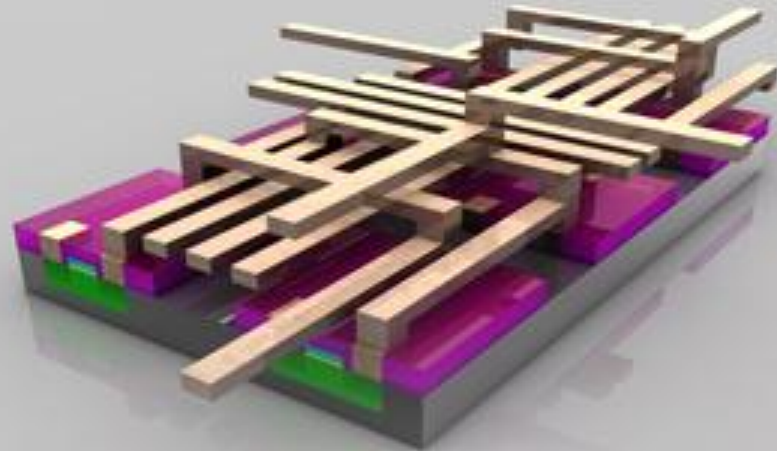
# Metal Layers



## *Polishing -*

*scale: transistor level (~50-200nm)*

The excess material is polished off.



## *Metal Layers - scale: transistor level (six transistors combined ~500nm)*

Multiple metal layers are created to interconnect (think: wires) in between the various transistors. How these connections have to be “wired” is determined by the architecture and design teams that develop the functionality of the respective processor (e.g. Intel® Core™ i7 Processor ). While computer chips look extremely flat, they may actually have over 20 layers to form complex circuitry. If you look at a magnified view of a chip, you will see an intricate network of circuit lines and transistors that look like a futuristic, multi-layered highway system.

# Wafer Sort Test / Slicing



## ***Wafer Sort Test -***

*scale: die level (~10mm / ~0.5 inch)*

This fraction of a ready wafer is being put to a first functionality test. In this stage test patterns are fed into every single chip and the response from the chip monitored and compared to "the right answer".



## ***Wafer Slicing -***

*scale: wafer level (~300mm / 12 inch)*

The wafer is cut into pieces (called dies).



## ***Discarding faulty Dies -***

*scale: wafer level (~300mm / 12 inch)*

The dies that responded with the right answer to the test pattern will be put forward for the next step (packaging).

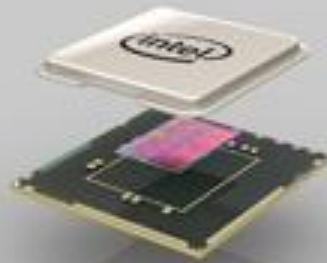
# Packaging



## *Individual Die -*

*scale: die level (~10mm / ~0.5 inch)*

This is an individual die which has been cut out in the previous step (slicing). The die shown here is a die of an Intel® Core™ i7 Processor .



## *Packaging -*

*scale: package level (~20mm / ~1 inch)*

The substrate, the die and the heatspreader are put together to form a completed processor. The green substrate builds the electrical and mechanical interface for the processor to interact with the rest of the PC system. The silver heatspreader is a thermal interface where a cooling solution will be put on to. This will keep the processor cool during operation.



## *Processor -*

*scale: package level (~20mm / ~1 inch)*

Completed processor (Intel® Core™ i7 Processor in this case). A microprocessor is the most complex manufactured product on earth. In fact, it takes hundreds of steps - only the most important ones have been visualized in this picture story - in the world's cleanest environment (a microprocessor fab) to make microprocessors.



# Class Testing / Completed Processor



## *Class Testing -*

*scale: package level (~20mm / ~1 inch)*

During this final test the processors will be tested for their key characteristics (among the tested characteristics are power dissipation and maximum frequency).

## *Binning -*

*scale: package level (~20mm / ~1 inch)*

Based on the test result of class testing processors with the same capabilities are put into the same transporting trays.

## *Retail Package -*

*scale: package level (~20mm / ~1 inch)*

The readily manufactured and tested processors (again Intel® Core™ i7 Processor is shown here) either go to system manufacturers in trays or into retail stores in a box such as that shown here.

# Manufacturing a SAW device

- *Now we focus on a specific method out of many many fabrication methods, and use it to show an example process for learning about how things are done*
- *A complete manufacturing program would require about four courses*
- *Consult the reading list to see where to go to learn more*

# Step 1: Base

- **There are many piezoelectric materials**
  - piezoelectric = pressure from electricity, a material that changes shape based on an applied voltage and vice-versa
  - fundamentally important material in
    - sensors, from quartz crystal microbalances to rain sensors
    - actuators, from cheap greeting card buzzers to picometer-accurate actuators
    - timers (“quartz” in quartz watches?)
- **Today we’ll choose lithium niobate**
  - single crystal media
  - strongly piezoelectric and pyroelectric
  - optically clear in visible light to soft UV



# Lithium niobate wafers

- **Geometry**
  - 0.5 mm thick, 100mm diameter (4”) with alignment notch perpendicular to x-axis
- **Crystal structure**
  - 128Y-X, Z, XY, X, 64Y-X, ...
  - we'll choose 128 Y-X
- **Surface finish and purity**
  - The surface finish may vary from as-cut, rough ground, to superoptical polish
  - Sometimes the surface finish is given in terms of roughness, mean in  $\mu\text{m}$  or  $\text{nm}$
  - Purity is important for consistency, beyond 99.99% is not unusual; *doped impurities are sometimes used for unique behaviors*
- **Yield**
  - How many devices do you need  $\times (1 + \text{failure rate in process}) = \text{devices per wafer} \times$   
**wafers to buy**
  - 100 devices  $\times$  10% failure rate = 110 devices; 110 devices / 10 devices per wafer = 11 wafers, about \$550 dollars

**Notes:**

**1.0 Orientations**

- 1.1 Wafer surface is normal to a direction  $127.85^\circ \pm 0.2^\circ$  rotated from the +Y through the +Z axis about the X axis.
- 1.2 Flats
  - 1.2.1 Primary flat is normal to the +X axis  $\pm 0.2^\circ$ .
  - 1.2.2 Secondary flat is  $90^\circ$  clockwise from the primary flat when viewing the polished face  $\langle +Z/-Y \rangle$ .

**2.0 Edge**

- 2.1 All edges rounded with  $R0.27 \pm 0.05\text{mm}$ .
- 2.2 No chips greater than 0.5mm in penetration and 1.0mm in length.

**3.0 Surfaces**

- 3.1 Side 1  $\langle +Z/-Y \rangle$  face  
Polished 10-5 scratch-dig with 1mm edge exclusion. No pits or scratches visible with reflected light and unaided eye.
- 3.2 Side 2  $\langle +Y/-Z \rangle$  face  
Ground,  $R_a 0.50\mu\text{m}-0.70\mu\text{m}$ .

**4.0 Flatness**

- 4.1 Warp  $< 50\mu\text{m}$ .
- 4.2 TTV  $< 25\mu\text{m}$ .

**5.0 Material**

- 5.1 Low angle grain boundaries up to  $0.3^\circ$  misorientation acceptable as determined by X-ray topography.
- 5.2 Curie temperature  $1142.3 \pm 1.9^\circ\text{C}$

side 1 polished  
 $127.85^\circ$  face

$32.5 \pm 2.0$

$\phi 100.0 \pm 0.2$

$\langle +X \rangle$

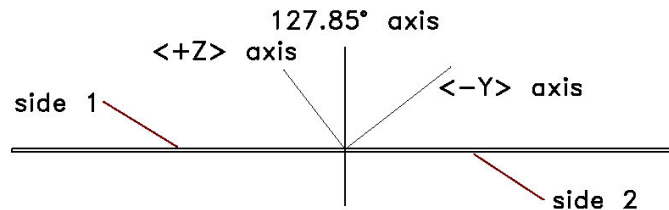
$14.0 \pm 2.0$

**For Reference Only**


$R0.27 \pm 0.05$

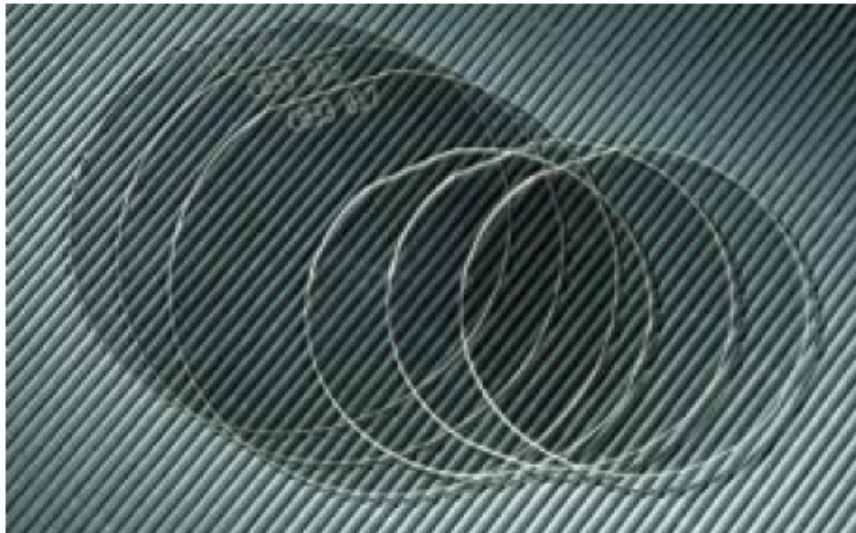
$0.500 \pm 0.020$

Wafer Edge Detail, 40X



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Material <b>Lithium Niobate</b>		DR. djundt	03-26-03	 <b>Crystal Technology, Inc.</b> An EPCOS Company
Unless otherwise specified, dimensions in mm		CHK.		
Tolerances		APPD.		Title: LNR4 100 $\phi$ x 0.5mm, 128° Po/Gr, +X FLT, TTV < 25 $\mu\text{m}$
Inches	Millimeters	Wafer Code: LNE128:100.050CP		Size: A
.X $\pm$ 0.1	X $\pm$ 0.5	Customer Approval:		Dwg. No: 97-01064-02
.XX $\pm$ 0.01	.X $\pm$ 0.25			Rev: A
.XXX $\pm$ 0.005	.XX $\pm$ 0.1			Scale: 1:1
.XXXX $\pm$ 0.0020	.XXX $\pm$ 0.05			Sheet 1 of 1
Angles $\pm 0.5^\circ$		DO NOT SCALE DRAWING		



Double-side polished lithium niobate optical wafers.



Single-side polished lithium niobate SAW wafers.

# Step 2: Clean

- So we get out the Windex and ...
- No, cleaning a wafer can require much more care than one might imagine
  - substrate
  - subsequent processing
  - condition the wafers arrived in
- Here,
  - the supplier provides oily wafers due to the polishing method
  - we want to place a thin metal coating on the substrate; metal substrates are notorious for flaking off of nonmetallics
  - piezoelectric substrates are sensitive to roughness, cracks, and rough handling
  - we are going to use a solvent to remove the oil followed by a *pirahna clean* to remove the oil, a DI water rinse to remove the pirahna clean products, and a N2 forced air dry to remove the DI water
  - ***atomically clean***



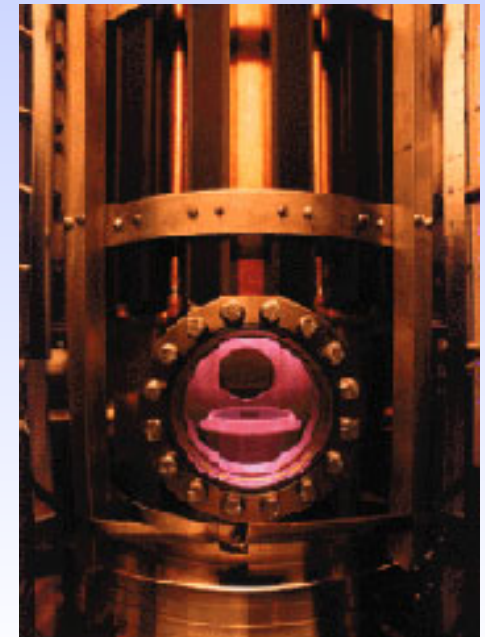
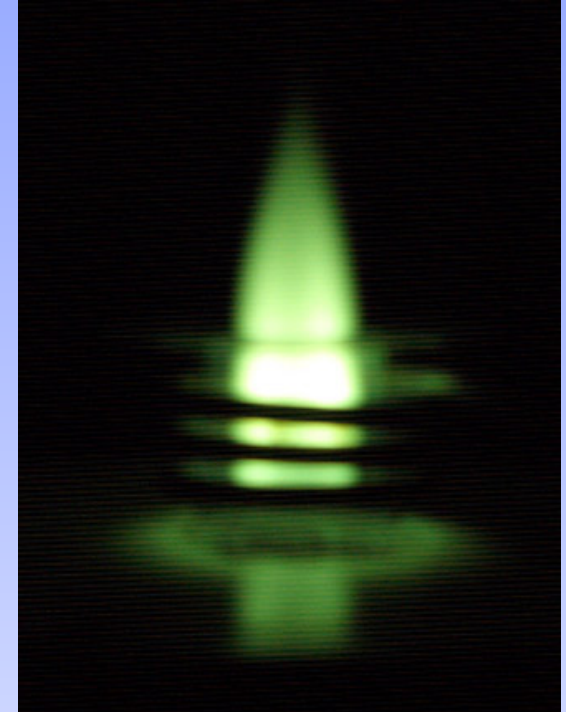
# *Pirahna clean*

- **Great process for cleaning non-metallic surfaces**
- **Process**
  - Measure 1 part (50 ml) 30% H<sub>2</sub>O<sub>2</sub> (Hydrogen Peroxide) in a 400 ml beaker.
  - Measure 5 parts (250 ml) H<sub>2</sub>SO<sub>4</sub> (Sulphuric Acid) in a beaker.
  - VERY slowly add acid to 30% H<sub>2</sub>O<sub>2</sub> (Hydrogen Peroxide)  
This mixture will self heat to about 100 deg. C
  - Place beaker on hotplate and heat to 130 deg. C
  - Place wafer in holder and set in acid for 7-10 minutes at 130 deg C
  - If mixture has cooled after use, it may be refreshed ONCE by heating to 100 deg. C and adding 30 ml. H<sub>2</sub>O<sub>2</sub> and heating to 130 deg again for use as above.
  - Rinse wafer with DI water (*do not let wafer dry ever!*)
  - Blow dry wafer center to edge with dry N<sub>2</sub>
- **Surface still not clean?**

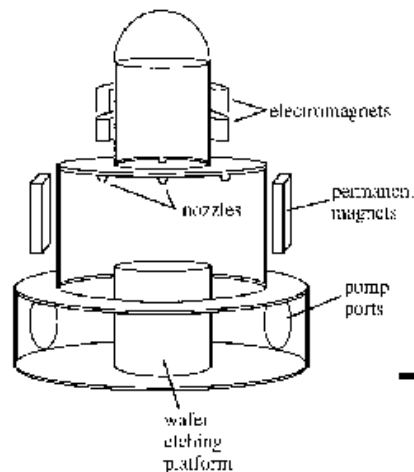


# Plasma etch

- A process in which the substrate is placed in a vacuum chamber with a small amount of reactive gas and where a powerful RF (1.5 -30MHz) EM field is induced to form a plasma
- The plasma impacts the substrate surface and anything on it, slowly eating it away
- Truly atomically clean, though rough surface (etch is random and anisotropic) may be a problem
- The form in the picture at right is coil inductive plasma, where an electric field is induced in the coil and about it in the surrounding gas
- The choice of gas depends on the substrate; here we will choose O<sub>2</sub> which will become atomic O in the plasma and react with chemical contaminants on the surface while leaving the lithium niobate mostly alone
- *Plasma etching affects hydrophobicity*
- *Plasma etching “activates” the surface chemically, so it is exceptionally easy to contaminate an etched surface---watch out!*



# EFFECT OF NOZZLE LOCATION ON THE NEUTRAL FLOW FIELD IN A PLASMA ETCH REACTOR



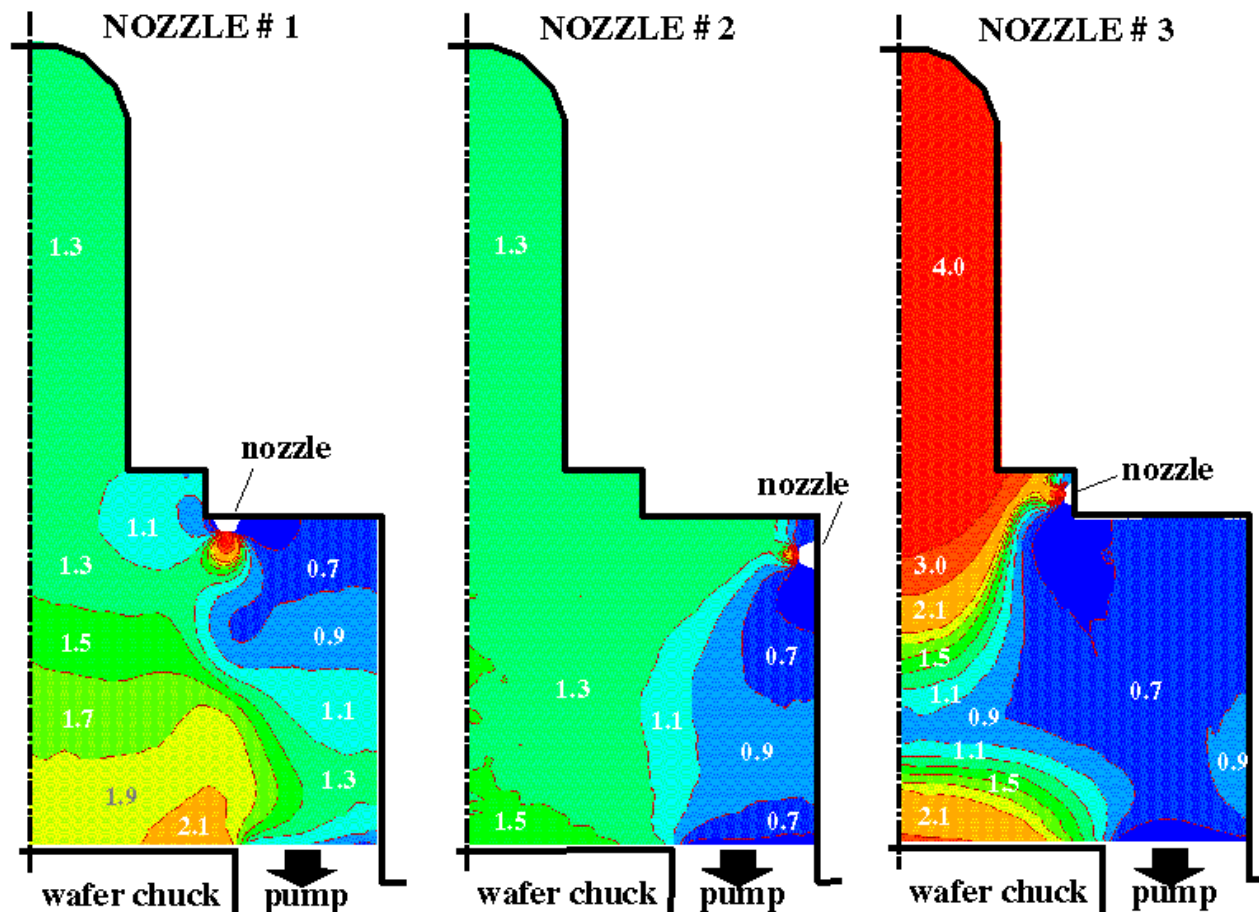
Density Contours ( $n \times 10^{20} \#/\text{m}^3$ )

DSMC Axisymmetric Simulation:

- $10^6$  particles

- IBM SP2: 8 processors

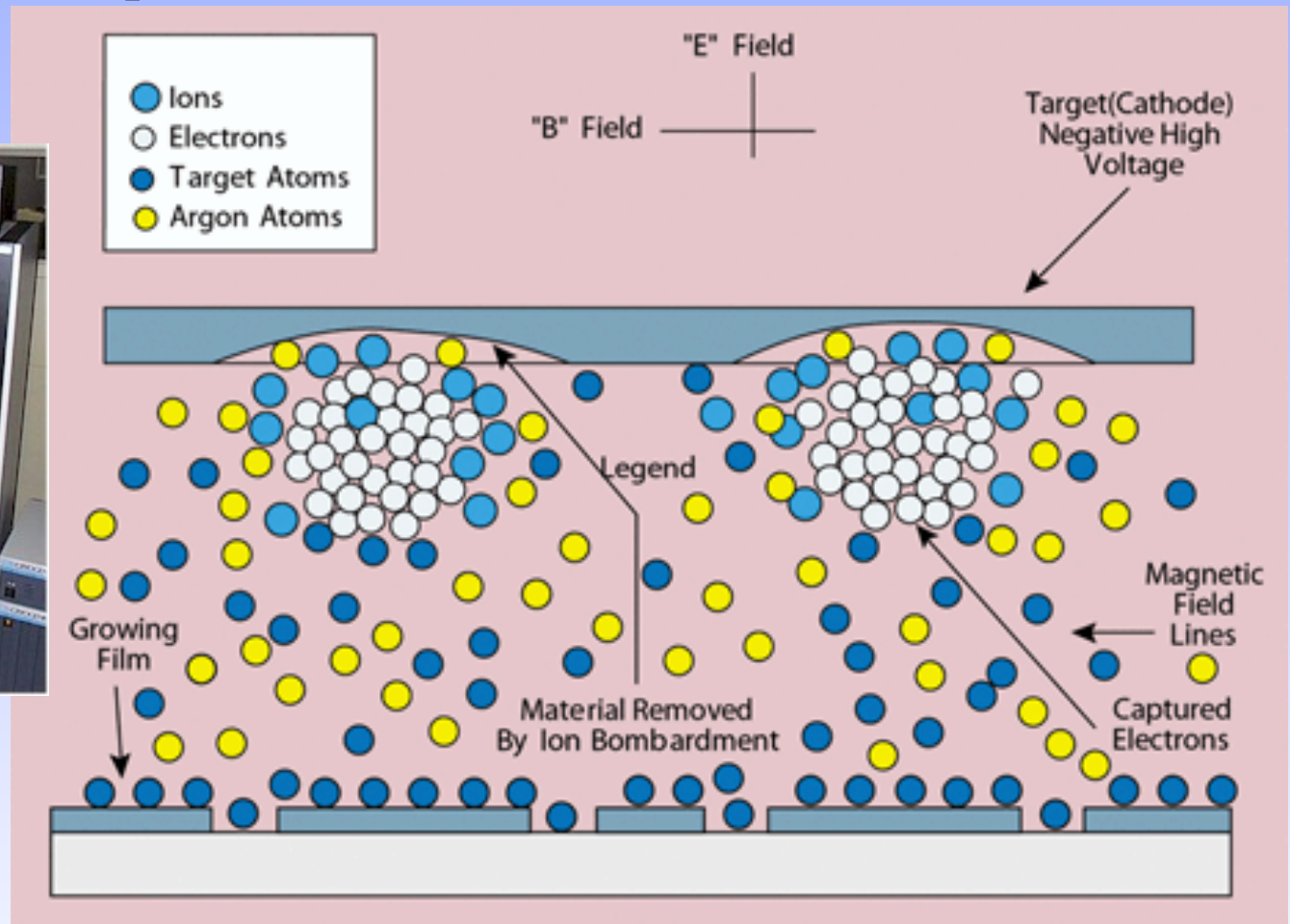
- neutral flow only:  $\text{Cl}_2$



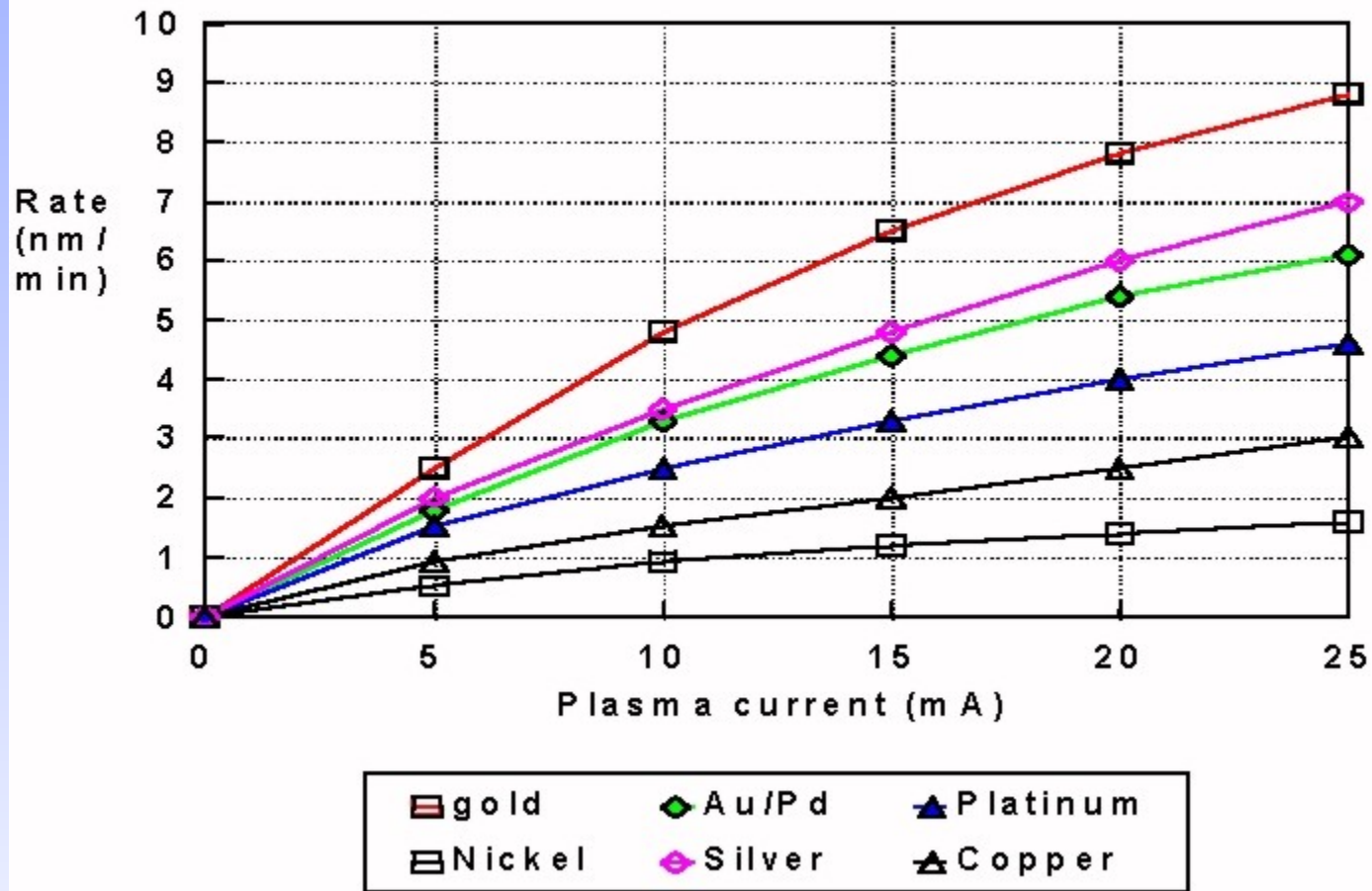
# Step 3: Treatment

- **We want patterned metal on the lithium niobate**
- **We could**
  - *Put down metal, then try and take part of the metal off later based on the pattern we want*
  - Put down a plastic layer, take part of that off, then put metal down; dissolving the remaining plastic would let us pop the metal left on the top of the plastic away (***lift off technique***)
- **Clean surface → good for metal adhesion → former technique**
- **Two good ways to get metal onto the surface**
  - Sputter deposition (\$\$\$, high quality, films to 2 um)
  - Vapor deposition (\$, good quality, films to 20 um)

# Sputter deposition

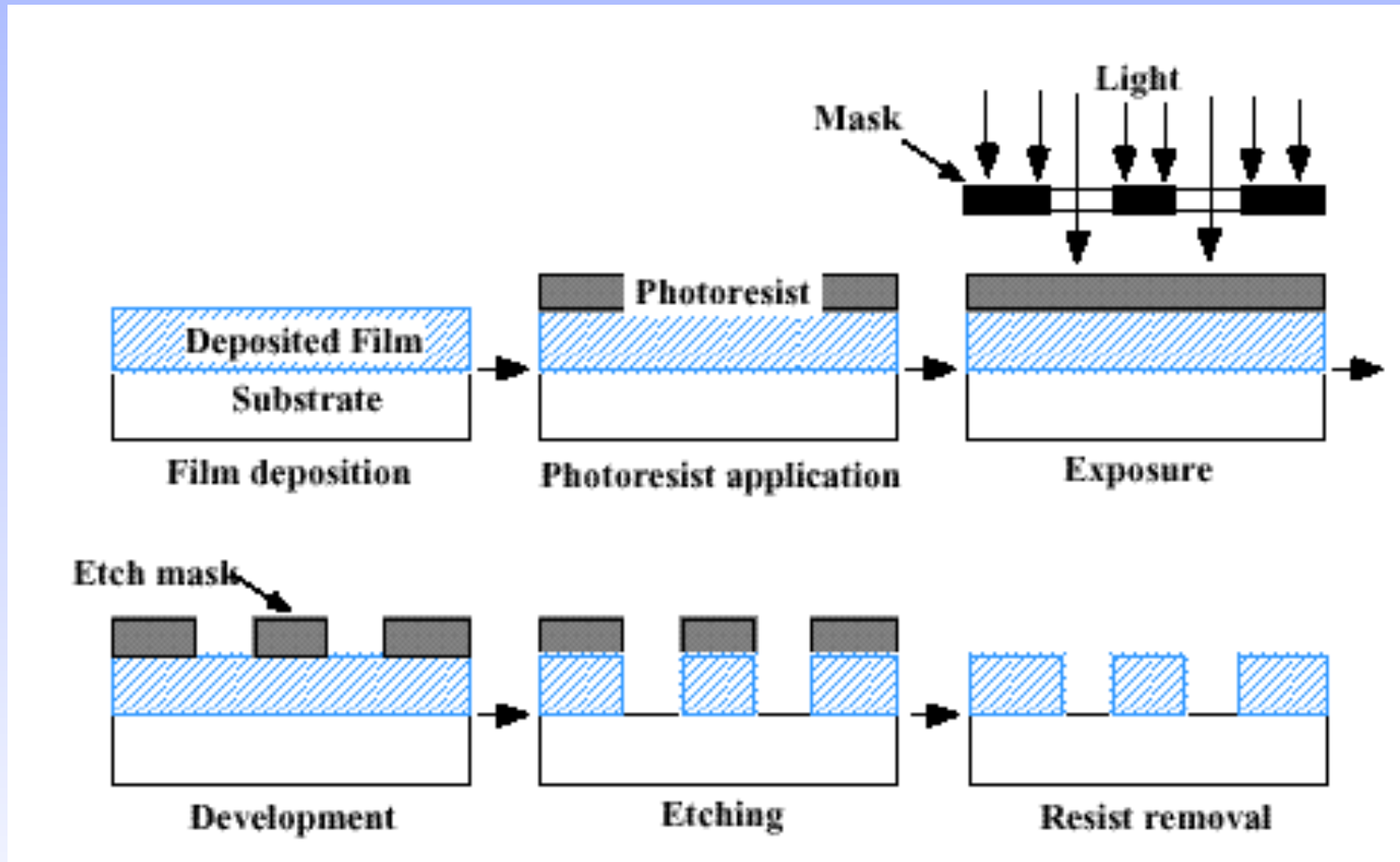


## Sputtering rate SC7620



# Photolithography (positive tone)

*Method of patterning structure on substrate*



# What do we want on the surface?

- **Choice of metals on the surface depend on**
  - adhesion to substrate
  - what we want to use the metal for (transmitting RF electric field)
  - ease of patterning
- **Adhesion to LN? *Titanium***
- **Conductivity? *Aluminum* or copper (Cu + Ti no good)**
- **Al is reactive → easy to pattern**
- **Ti is *not* → *big problem, but only reasonable choice for LN***
- ***4 nm Ti + 1 um Al* → *one then the other, two-stage sputtering system***
- **Best choice: sputter etch to clean then sputter deposit Ti for 15 sec followed by sputter deposit Al for 2-3 hours**

# Step 3 round 2: Polymer

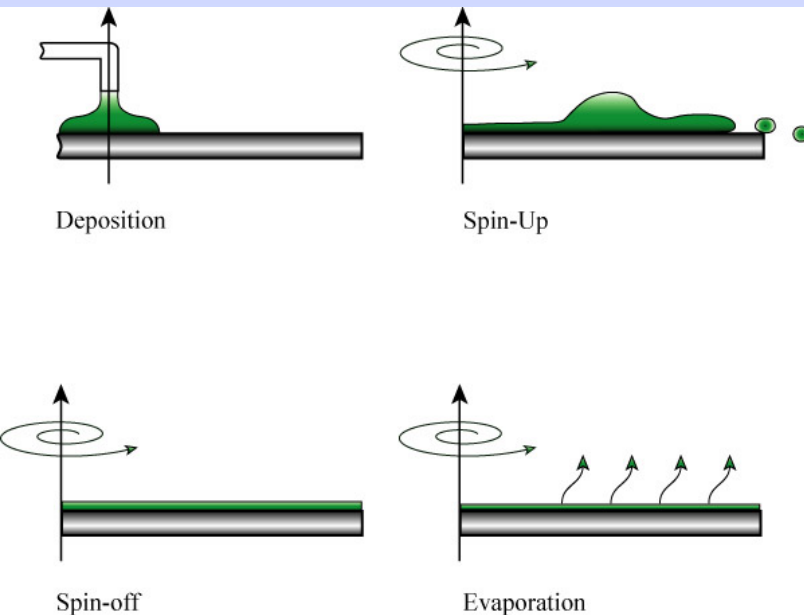
- **Polymer coat for patterning**
  - To form a shape on the substrate by removing selected sections of the metal coating
  - Requires coating that is sensitive to UV radiation' *photoresist*
- **Many different kinds of photoresist**
  - viscosity
  - radiation sensitivity (wavelength and time)
  - positive versus negative tone resist
  - final thickness → resolving power
- **Two principal methods**
  - Spin-coating
  - Dip-coating
- **Spin-coating generally provides more consistent coating thicknesses for thin polymer films**
- **Seminal paper: Meyerhofer, J. Appl. Phys. 49 (1978) 3993**
- **We want 50 um feature size, so divide that by 2 and arrive at 25 um polymer coat thickness; AZ4562 (next page) is a good choice**





# Spin-coat process and photoresists

- Here we'll apply the resist
- Spin-up at 100 rpm for 20 sec
- Spin-off at 4500 rpm for 60 sec
- Gives a 10 um thick coating
- Followed by "rest" evaporation and bake at 90C for 15 minutes...to allow volatile carrier to evaporate and polymer to densify
- Pyroelectric substrate, so bake cycle requires 2 hr 15 min to avoid arcing

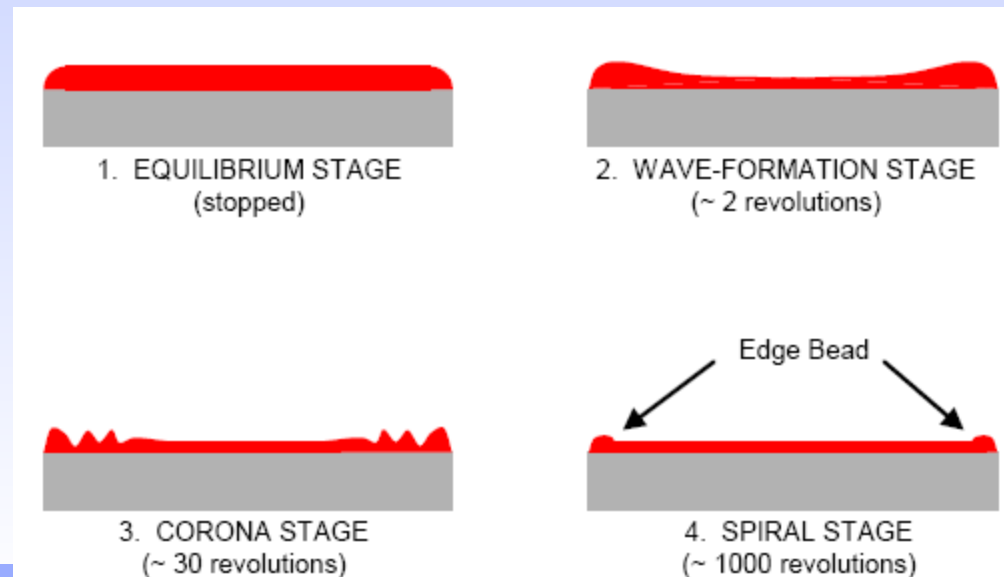


attainable resist thickness range (micron)		0.5	1.0	1.5	2.0	2.5	3.0	3.5	4	5	6	8	10	15	20	25	50	100	
standard/ wet chemical etching	AZ <sup>®</sup> 1505	Green																	
	AZ <sup>®</sup> 1512HS	Green	Green																
	AZ <sup>®</sup> 1514H	Green	Green	Green															
	AZ <sup>®</sup> 1518	Green	Green	Green	Green														
	TI 35E	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green
TI Duran	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green
thick resists	AZ <sup>®</sup> 4533																		
	AZ <sup>®</sup> 4562																		
	AZ <sup>®</sup> 9260																		
	TI Plating																		
TI xLift																			
dry chemical etching	AZ <sup>®</sup> 6612																		
	AZ <sup>®</sup> 6624																		
	AZ <sup>®</sup> 6632																		
	TI 35ES																		
high resolution	AZ <sup>®</sup> MIR701																		
	TI 09XR																		
	AZ <sup>®</sup> 9260																		
image reversal/ lift-off	TI 09XR																		
	AZ <sup>®</sup> 5214E																		
	TI 35E/ES																		
	TI Spray																		
	TI Duran																		
	TI Plating																		
	TI xLift																		
negative resist	AZ <sup>®</sup> nLOF																		

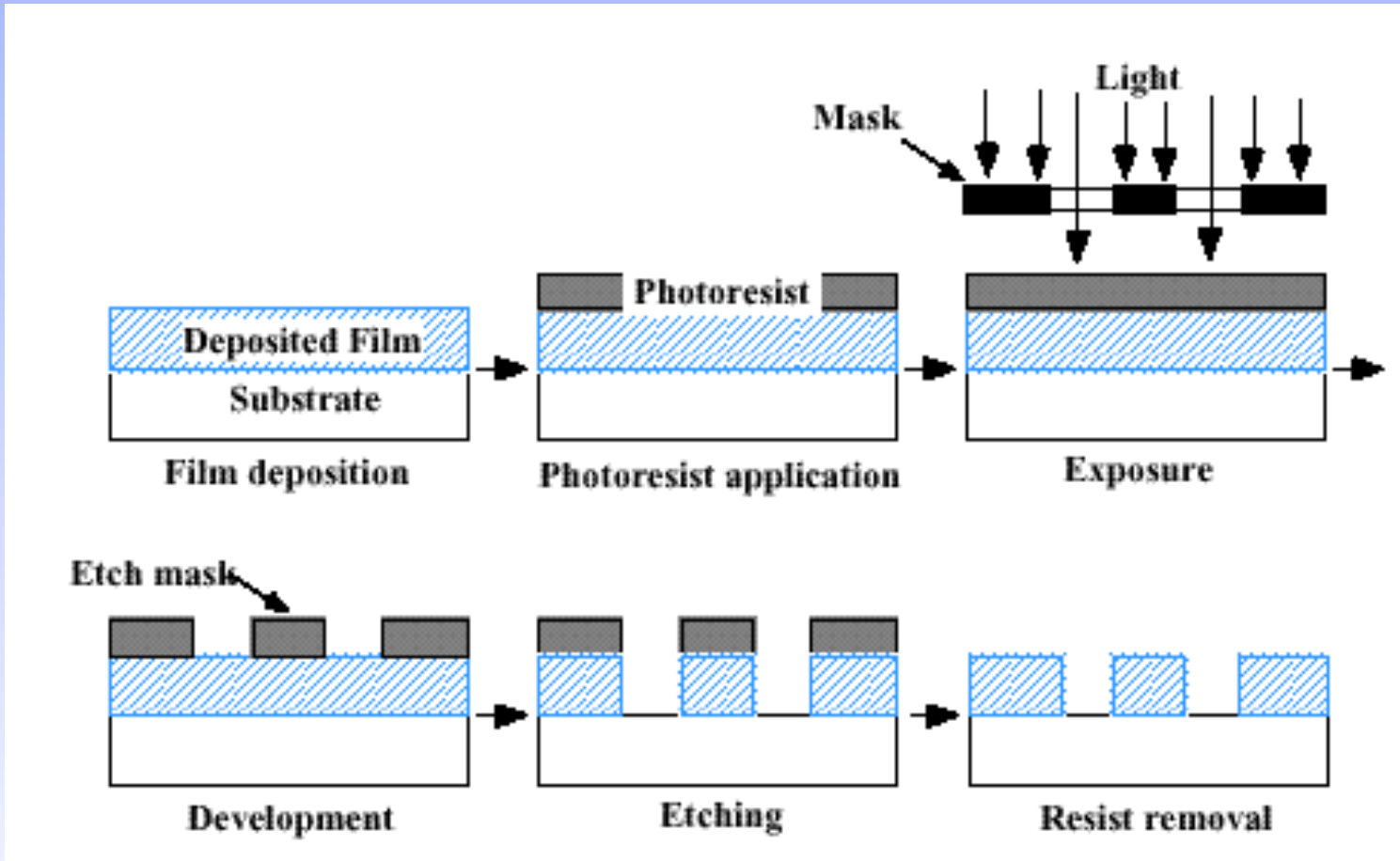
Legend: green: standard yellow: dilution/multiple coating

# Spin-coating cont'd

- Wafer is held on a spinner chuck by vacuum and resist is coated to uniform thickness by spin coating
- Resist thickness is set by:
  - primarily resist viscosity
  - secondarily spinner rotational speed
- Resist thickness is given by  $t = kp^2/w^{1/2}$ , where
  - **k = spinner constant, typically 80-100**
  - **p = resist solids content in percent**
  - **w = spinner rotational speed in rpm/1000**

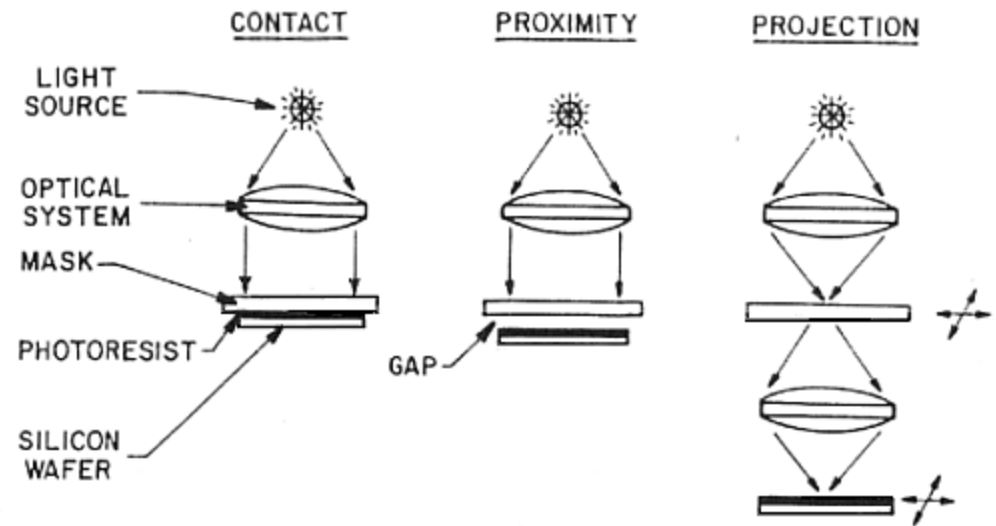


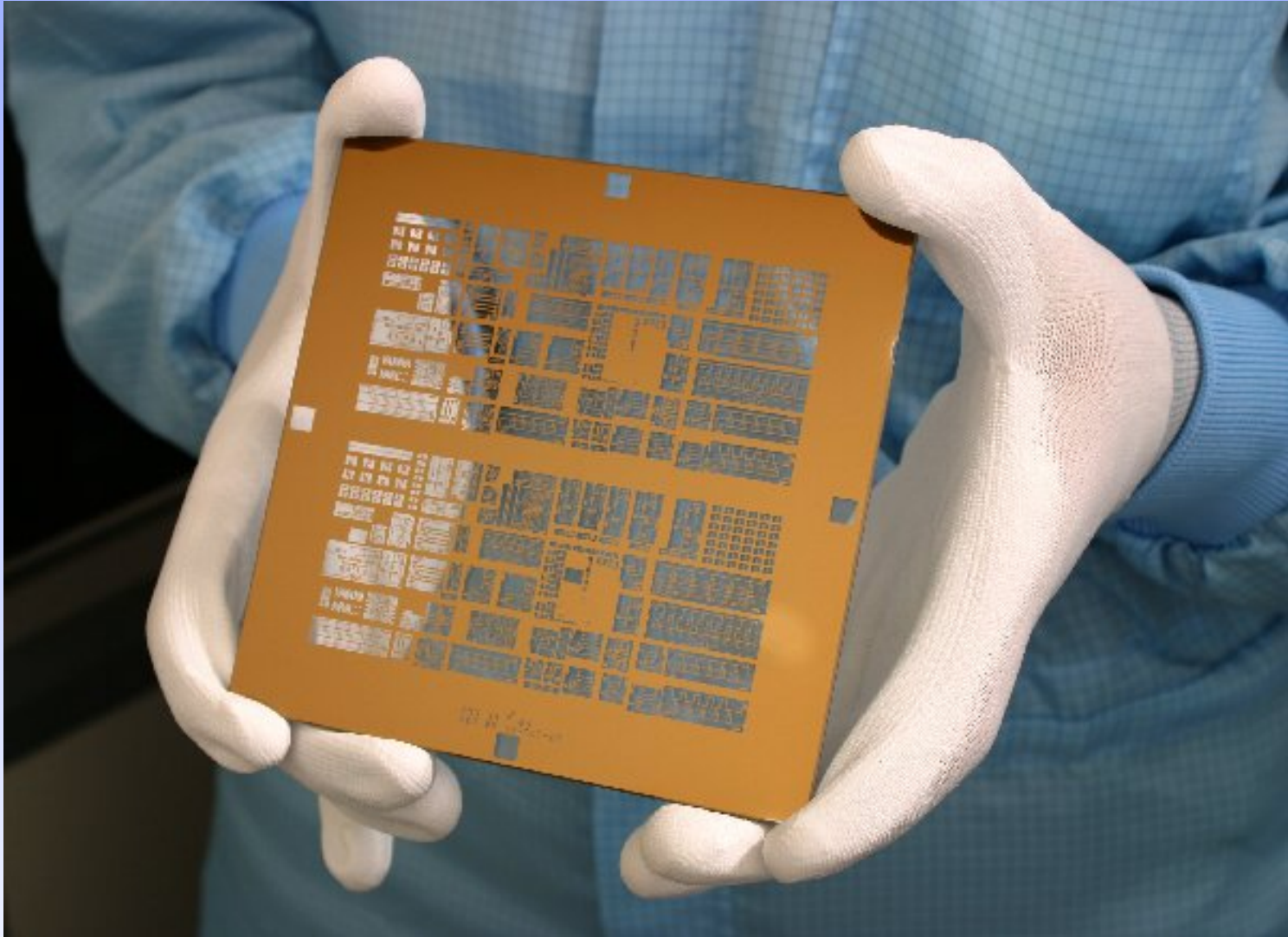
# Photolithography (positive tone)

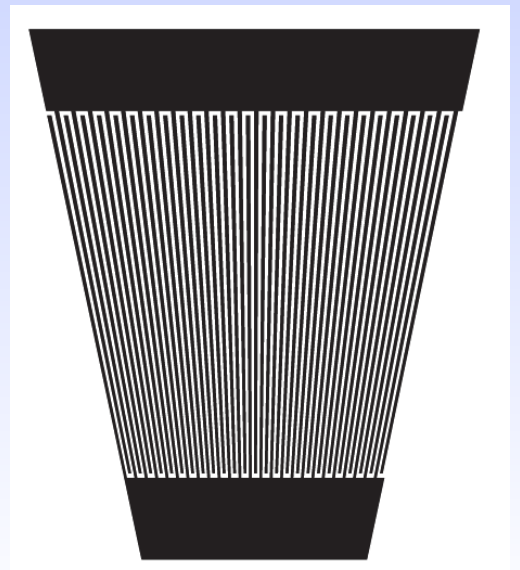
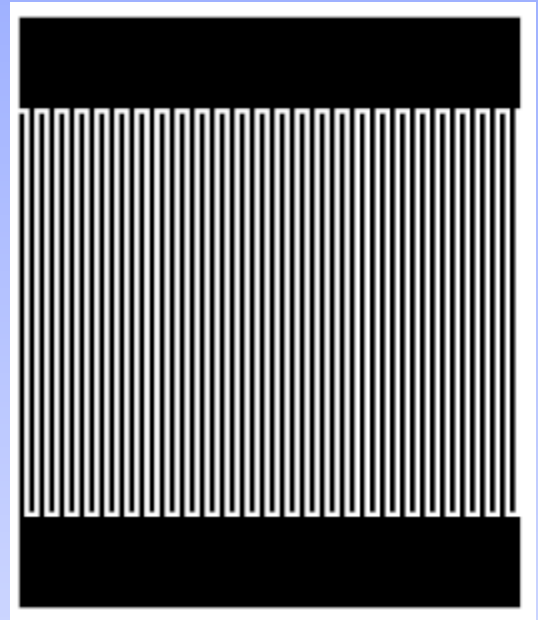
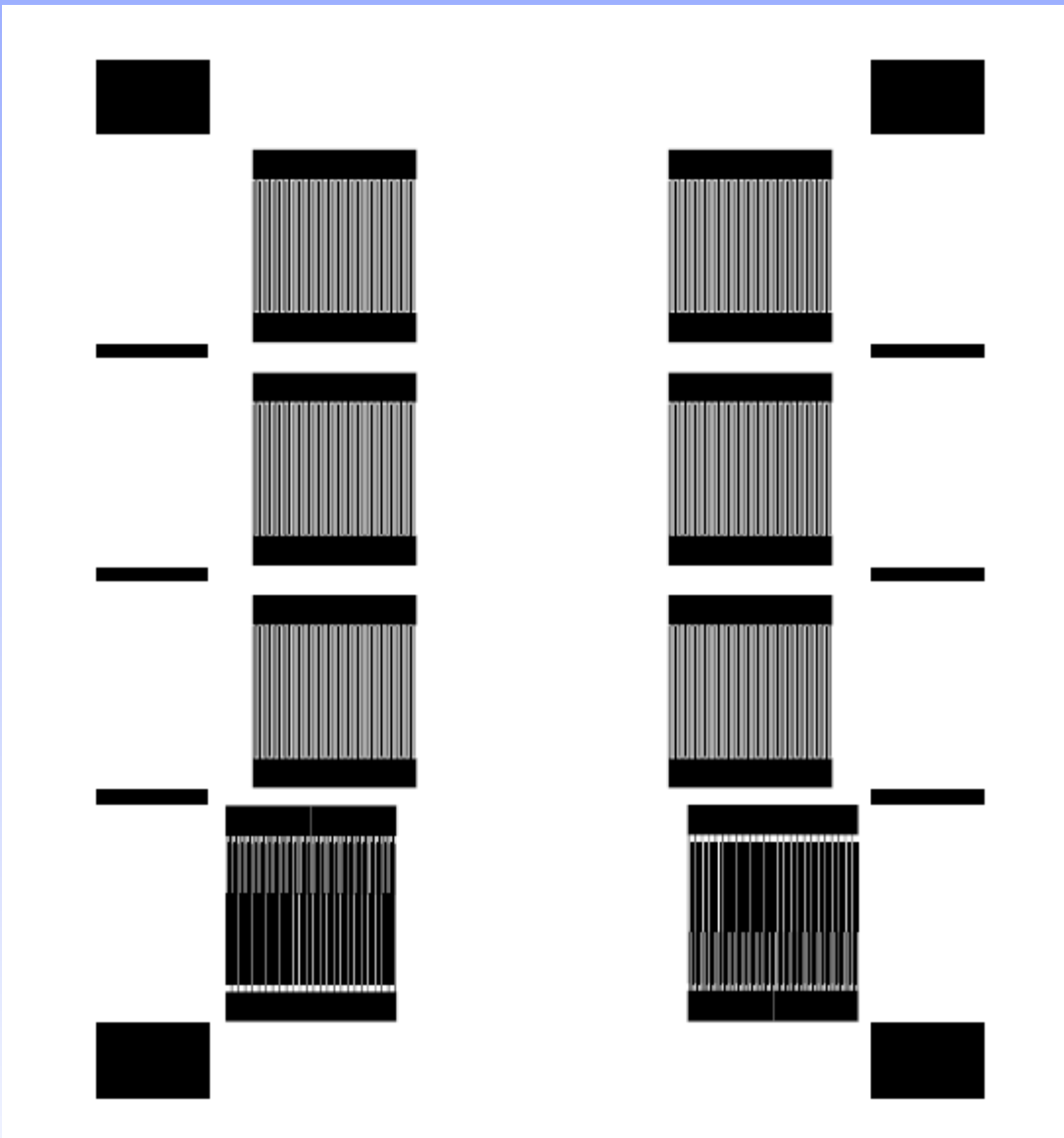


# Patterning: Photolithography

- A light source (here UV) is used to *expose* part of the polymer photoresist left on the surface and cause it to *either polymerize or depolymerize*
- The pattern is defined by the *mask*, produced by electron beam lithography or in cheap cases, a linotype laser printer from a CAD file onto a transparency
- Here we need accuracy, so a 5" x 1 mm thick quartz plate will be used, with a stainless steel mask pattern

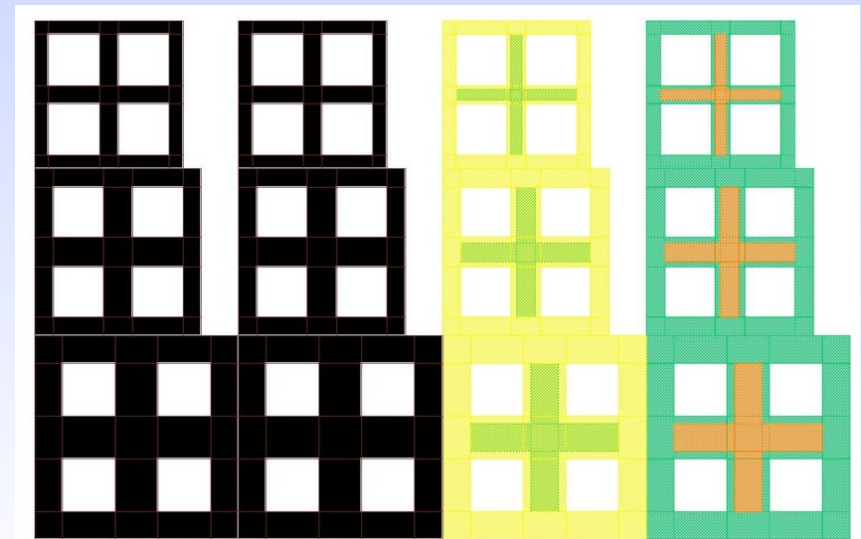
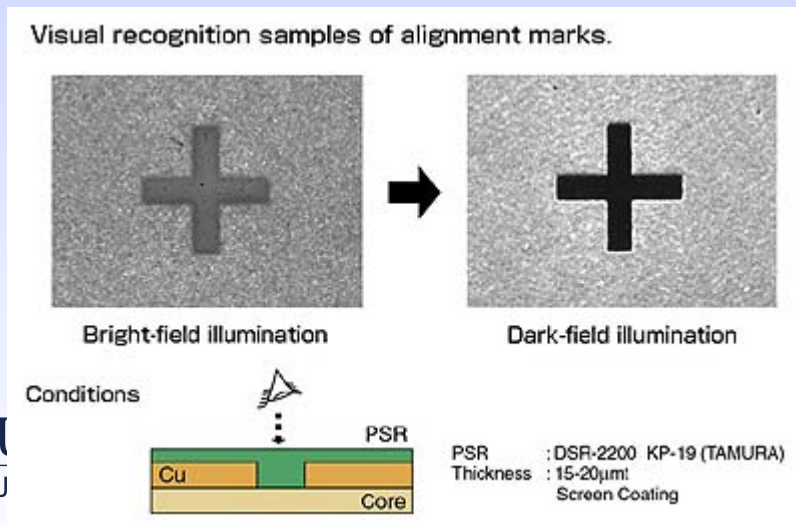


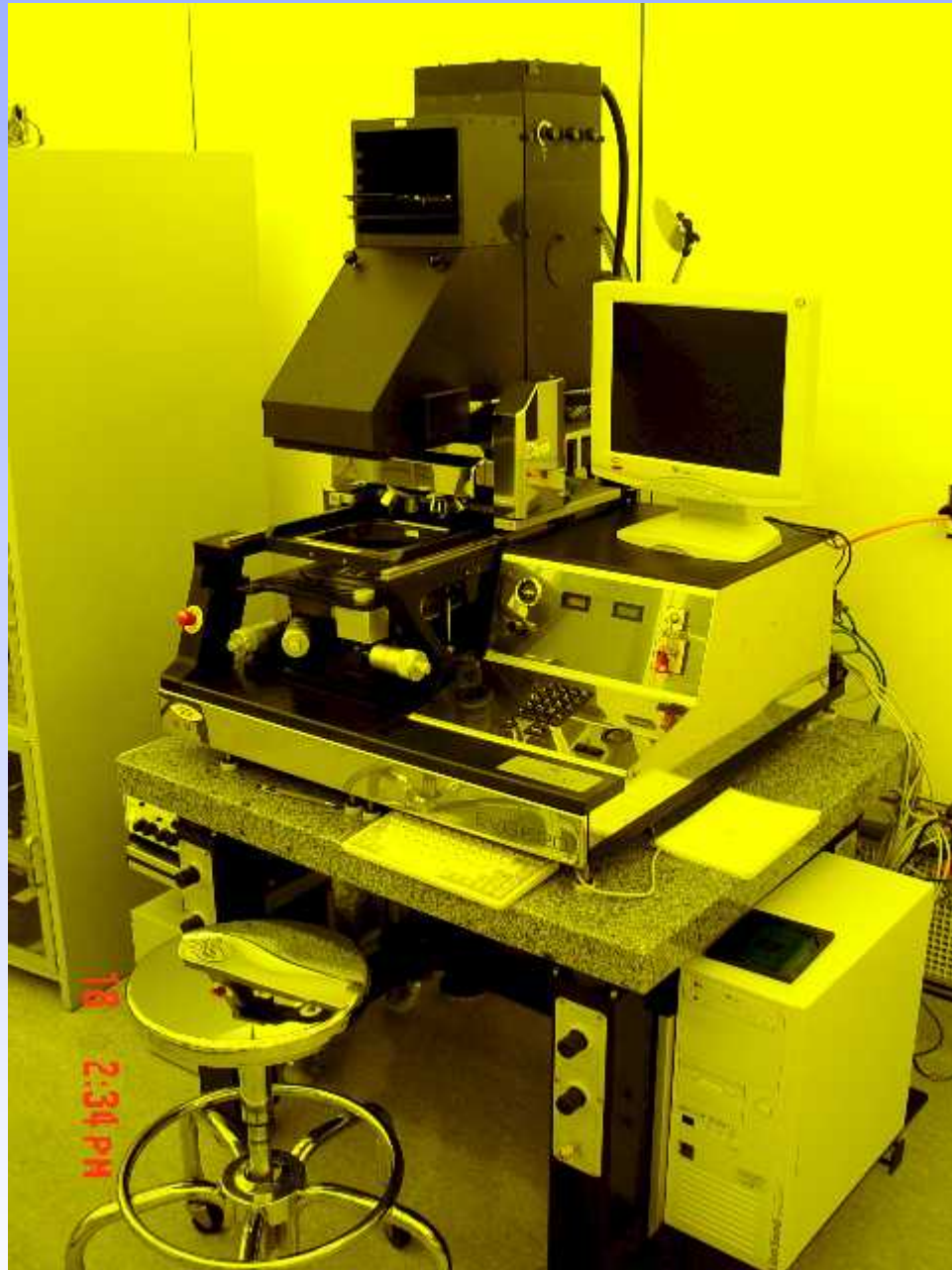




# Mask Aligner

- The system used to perform the UV exposure is called a *mask aligner*
- It holds the substrate and mask together with an alignment system to permit multiple exposures for many layers
  - CPU chips may have >20 layers in Si/SiO/doped Si
  - Requires registration marks for multiple exposures



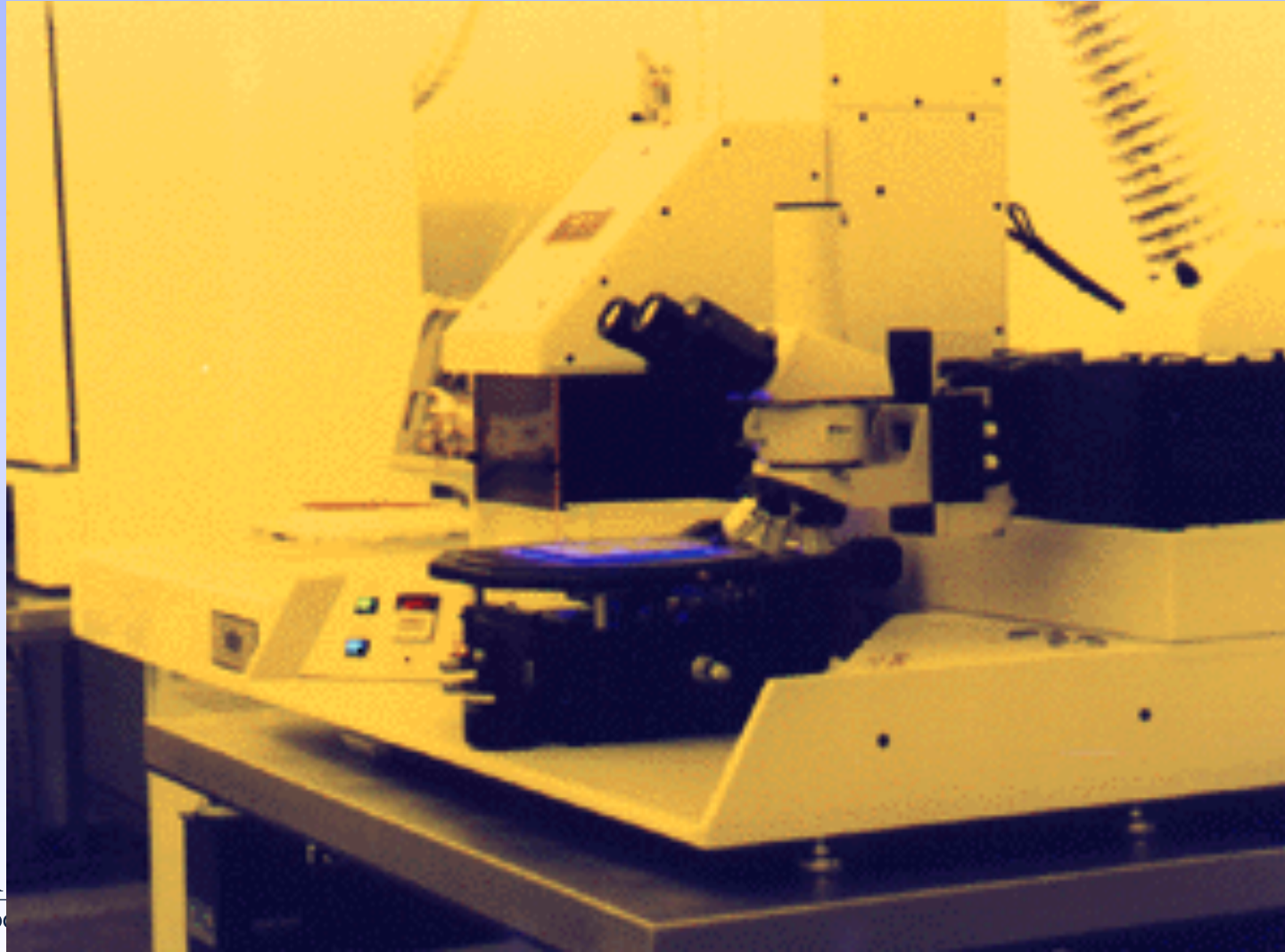






# Mask aligner emitting UV radiation

*(dangerous to eyes and skin)*



(x,y,θ) alignment of mask to substrate



uniform UV exposure illumination



chrome on glass photomask



photoresist (PR)



substrate wafer

latent image created in photoresist after exposure

wet chemical development



**NEGATIVE PHOTORESIST**

Photoresist is photopolymerized where exposed and rendered insoluble to the developer solution.

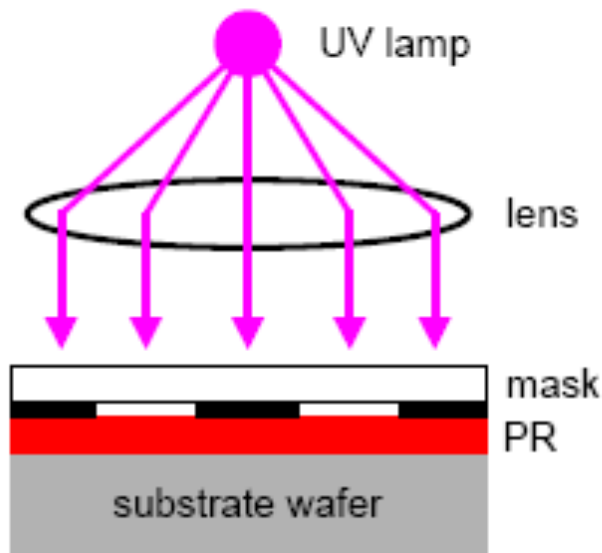


**POSITIVE PHOTORESIST**

Exposure decomposes a development inhibitor and developer solution only dissolves photoresist in the exposed areas.

# Alignment and Exposure Hardware - 1

CONTACT ALIGNER



2 operating modes:  
contact for expose;  
separate for align.

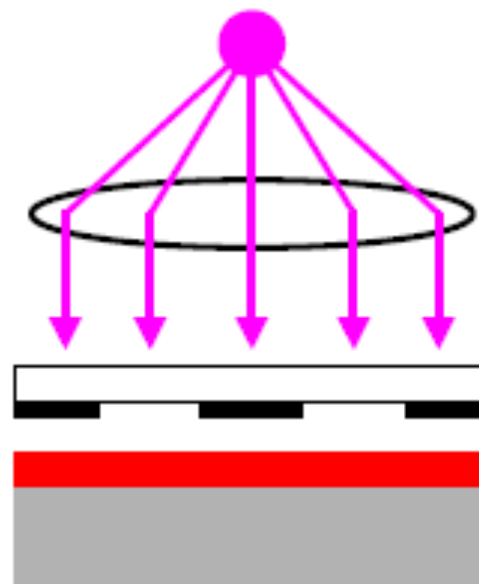
Examples:

Kaspar 17A

Oriel

Karl Suss MJB3

PROXIMITY ALIGNER

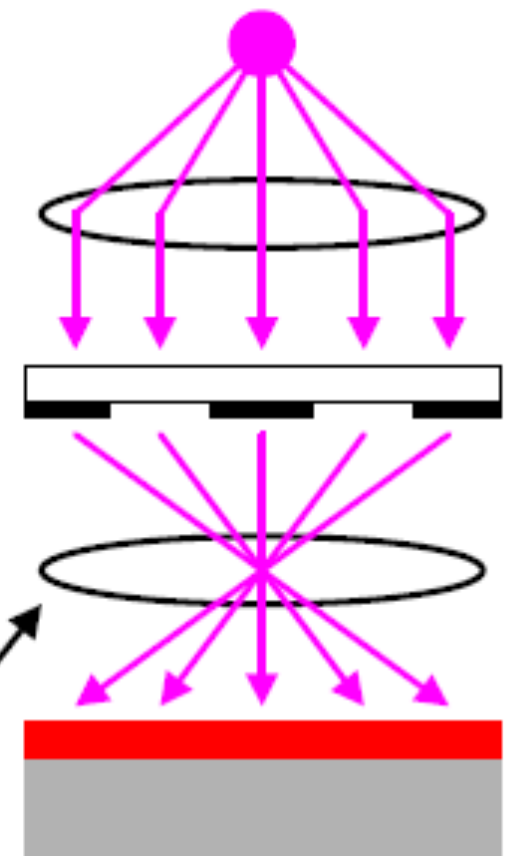


less wear on mask, but  
poorer image than from  
a contact aligner.

Examples:

Kaspar-Cobilt

PROJECTION ALIGNER



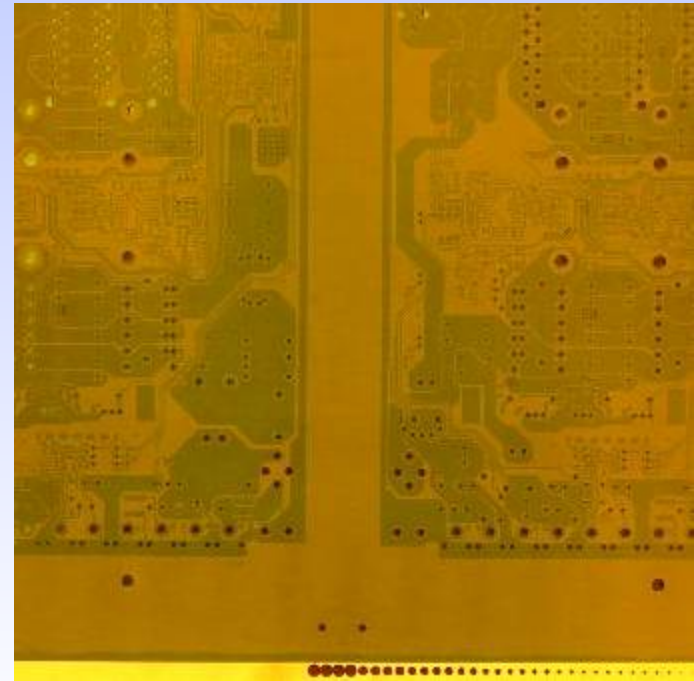
Examples:

Perkin-Elmer Micralign

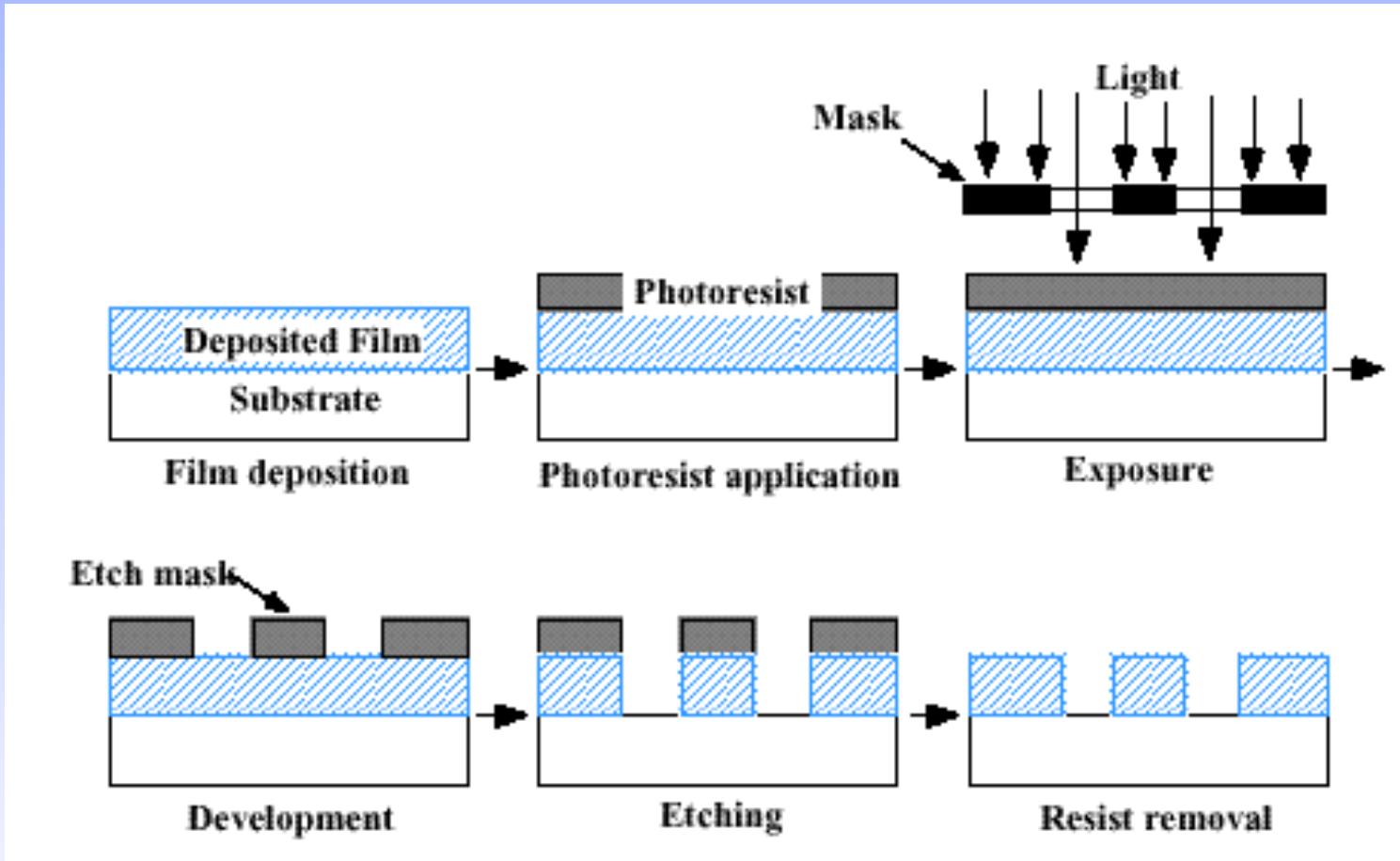
Projection systems use imaging optics  
in between the mask and the wafer

# Develop Polymer Photoresist

- Once the photoresist has been exposed, it must “rest” for a few minutes (depending on the resist)
- A post-bake may be used to harden the photoresist post-exposure (here, we won’t due to hassle of pyroelectricity of substrate)
- Subsequently, the photoresist must be “developed” to remove the exposed (positive tone) or unexposed (negative tone) resist
- Here, the exposed regions will be removed



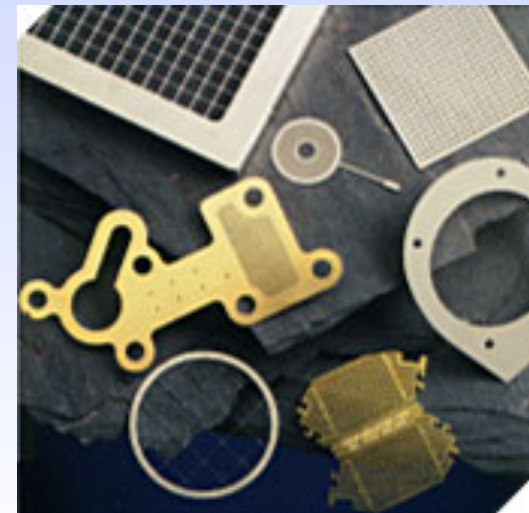
# Photolithography (positive tone)



# Etch metals according to pattern

- What etches metals but not a polymer or ceramic?
- What etches aluminum?
- What etches titanium? (tough question)
- Polar acids generally etch metals but not polymers and ceramics
- Dry etch (RIE plasma etch or ion milling) etches *everything* but \$  
\$\$

Etch Rate (R)	Rate of film removal, typically 1000 A/min.
Etch Uniformity (U)	% change in etch rate across a wafer, lot, etc
Selectivity( $S_{fm}$ , $S_{fs}$ )	Ratio of the etch rate of various materials e.g. Film to PR $S_{fm}$ : Film to mask selectivity; $S_{fs}$ : Film to substrate selectivity
Anisotropy, A	Measure of directionality of the etch. A=1 corresponds to perfect anisotropic etch A=0 corresponds to isotropic etch
Undercut	Measure of the lateral extent of the etch per side
Substrate Damage	Physical and/or chemical damage of the substrate.



# Sample metal etching chemicals

**Aluminum** - “Aluminum Etchant Type A” from Transene Co., Inc. is a mixture of phosphoric acid, acetic acid and nitric acid. Etch Rate is about 1 min for 2000 Å.

For multilayer metal processes it is often necessary to etch through an insulating interlevel dielectric. When the underlying layer is aluminum and the insulating layer is glass the preferred etchant is 5 parts BOE and 3 parts Glycerin. (straight BOE etches aluminum)

**Copper** - Ferric Chloride or mix Etchant from 533 ml water, add 80 ml Na<sub>2</sub>S<sub>2</sub>O<sub>3</sub>, Sodium Persulfate, (white powder, Oxidizer), prepare in glass pan, place pan on hot plate and heat to 50 C (plate Temp set at 100 C) Etch Rate ~ 1.66 µm/min  
Copper Coated Board about 30 min.

**Platinum** - 7ml HCl, 1ml HNO<sub>3</sub>, 8 ml H<sub>2</sub>O at 85 C approximate etch rate 450 Å/min.

**Chromium** - CR-9 Etch, Cyantek Corp.

**Gold** - Gold Etch.



# Titanium etching?

- **Have to go to the literature...**

JOURNAL OF MICROELECTROMECHANICAL SYSTEMS, VOL. 12, NO. 6, DECEMBER 2003

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## Etch Rates for Micromachining Processing—Part II

Kirt R. Williams, *Senior Member, IEEE*, Kishan Gupta, *Student Member, IEEE*, and Matthew Wasilik

Etch	Aluminum Evap	Al + 2% Si Sputtered	Titanium Sputtered	Vanadium Evap	Niobium Ion-Mill	Tantalum Evap	Tantalum Ion-Mill	Chromium Evap	Chromium Ion-Mill	Patterned Cr on Au Evap
Si Iso Etch	60	400	300	9600	79	5.8	5.3	R 8.8	-	< 2.3
KOH	12,900	F	soft	< 12	3.2	S	2.8	4.2	-	0
10:1 HF	W	250	1100	S	S	S	S	S	S	-
5:1 BHF	11	140	W	< 2	0	S	R 0	0	< 0.3	P
Pad Etch 4	1.9	R < 15	< 2	S	S	S	S	S	S	-
Phosphoric	> 500	980	-	-	0	-	0	100	-	-
Al Etch A	530	660	0	-	-	-	-	T 0	-	1.0
Ti Etch	150	240	1100	-	-	-	-	0	S	-
CR-7	3.8	S	< 2	60	R 0	S	< 0.7	170	150	110
CR-14	0	0.8	< 2	15	-	-	-	93	W	120
Moly Etch	> 20	-	-	-	-	-	-	R 0	-	-
H <sub>2</sub> O <sub>2</sub> 50°C	T 0	0.25	-	-	-	-	-	110	W	-
Cu FeCl <sub>3</sub> 200	35	W	-	-	-	-	-	0.053	S	-
Cu APS 100	< 0.3	-	-	-	-	-	-	0	S	-
Dil. Aqua regia	600	W	< 0.5	-	0	S	< 2	0	S	-
AU-5	-	-	-	-	-	-	-	0	S	-
NiCr TFN	> 46	-	-	-	-	-	-	> 170	W	W
Phos+Sulf	W	W	-	-	-	-	-	I > 500	-	-
Piranha	> 5200	W	240	-	6.3	S	T 0	> 16	5.7	R 0
Microstrip	-	-	-	-	-	-	-	-	-	-
Acetone	S	0	0	S	S	S	S	S	S	S
Methanol	S	S	S	S	S	S	S	S	S	S

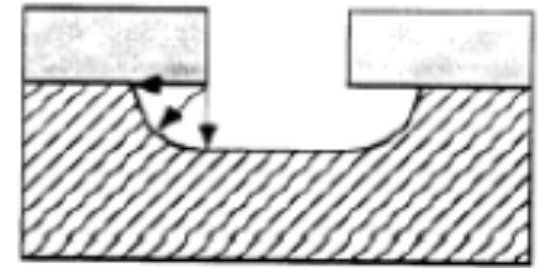
Numbers are in nm/min

Etch	Aluminum Evap	Al + 2% Si Sputtered	Titanium Sputtered	Vanadium Evap	Niobium Ion-Mill	Tantalum Evap	Tantalum Ion-Mill	Chromium Evap	Chromium Ion-Mill	Patterned Cr on Au Evap
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KOH	12,900	F	soft	< 12	3.2	S	2.8	4.2	-	0
10:1 HF	W	250	1100	S	S	S	S	S	S	-
5:1 BHF	11	140	W	< 2	0	S	R 0	0	< 0.3	P
Pad Etch 4	1.9	R < 15	< 2	S	S	S	S	S	S	-
Phosphoric	> 500	980	-	-	0	-	0	100	-	-
Al Etch A	530	660	0	-	-	-	-	T 0	-	1.0
Ti Etch	150	240	1100	-	-	-	-	0	S	-
CR-7	3.8	S	< 2	60	R 0	S	< 0.7	170	150	110
CR-14	0	0.8	< 2	15	-	-	-	93	W	120
Moly Etch	> 20	-	-	-	-	-	-	R 0	-	-
H <sub>2</sub> O <sub>2</sub> 50°C	T 0	0.25	-	-	-	-	-	110	W	-
Cu FeCl <sub>3</sub> 200	35	W	-	-	-	-	-	0.053	S	-
Cu APS 100	< 0.3	-	-	-	-	-	-	0	S	-
Dil. Aqua regia	600	W	< 0.5	-	0	S	< 2	0	S	-
AU-5	-	-	-	-	-	-	-	0	S	-
NiCr TFN	> 46	-	-	-	-	-	-	> 170	W	W
Phos+Sulf	W	W	-	-	-	-	-	I > 500	-	-
Piranha	> 5200	W	240	-	6.3	S	T 0	> 16	5.7	R 0
Microstrip	-	-	-	-	-	-	-	-	-	-
Acetone	S	0	0	S	S	S	S	S	S	S
Methanol	S	S	S	S	S	S	S	S	S	S

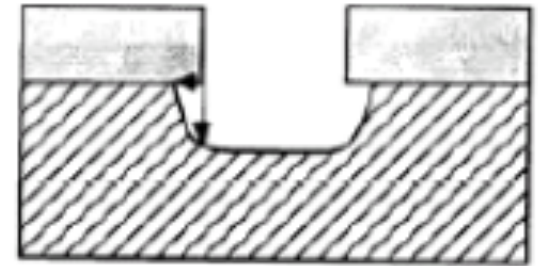
Numbers are in nm/min

# Etch Anisotropy

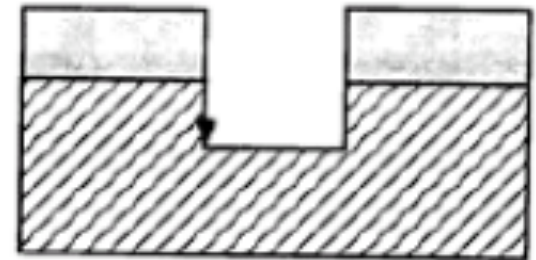
Etch Directionality	Measure of relative etch rates in different directions usually vertical vs. lateral
Isotropic Etching	Etch rates are same in all directions. It is usually related to chemical processes
Anisotropic Etching	Highly directional etching with different etch rates in different directions. It is usually related to physical processes such as ion bombardment and sputtering



a. isotropic



b. anisotropic



c. completely anisotropic

# HF etch

- Only realistic method for wet etching
- Problem? HF is deadly poisonous
- **MSDS: HYDROFLUORIC ACID #: H3994**
- Emergency Overview



**POISON! DANGER! CORROSIVE. EXTREMELY HAZARDOUS LIQUID AND VAPOR. CAUSES SEVERE BURNS WHICH MAY NOT BE IMMEDIATELY PAINFUL OR VISIBLE. MAY BE FATAL IF SWALLOWED OR INHALED. LIQUID AND VAPOR CAN BURN SKIN, EYES AND RESPIRATORY TRACT. CAUSES BONE DAMAGE. REACTION WITH CERTAIN METALS GENERATES FLAMMABLE AND POTENTIALLY EXPLOSIVE HYDROGEN GAS.**

- **General:** For burns of moderate areas, ... admission to a critical care unit should be considered. ... Burns beneath the nail may require splitting the nail and application of calcium gluconate to the exposed nail bed. ... **Eyes:** Irrigation may be facilitated by use of Morgan lens or similar ocular irrigator, using 1% aqueous calcium gluconate solution [50ml of calcium gluconate 10% in 500 ml normal saline].
- **AN ALTERNATIVE FIRST AID PROCEDURE:** The effect of HF, i.e. onset of pain, particularly in dilute solutions, may not be felt for up to 24 hours. It is important, therefore, that persons using HF have immediate access to an effective antidote even when they are away from their work place in order that first aid treatment can be commenced immediately.
- We recommend that any person in contact with HF should carry, or have access to a tube of HF Antidote Gel at all times; ideally with one tube at the work place, one on the person and one at home.

# Appropriate etch here?

- Minimum HF to get the job done
- 1:20 H<sub>2</sub>O:HF is sufficient
- Approximately 2 min for Al, 5 sec for Ti
- Immediately followed by DI water rinse x 2 and N<sub>2</sub> air dry under fume cupboard
- Followed by stripping of last photoresist remaining on wafer: acetone, 30 seconds
- DI H<sub>2</sub>O clean followed by N<sub>2</sub> dry
- ***Done***